A 5GHz LC VCO with Extended Linear-Range Varactor in Purely Digital 0.15um CMOS Process

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Abstract — **MOSFET varactors with two different threshold voltages are used for extending linear tuning range of a voltage controlled oscillator (VCO). This method is suitable for VCOs implemented in purely digital CMOS processes where MIM-capacitors are not available and only MOS transistors can be used for tuning element. The effectiveness of this technique is demonstrated in a 5GHz LC VCO with divide-by-2, output buffer, and integrated low-dropout voltage regulator. The VCO consumes 4mA of current and achieves a tuning range of 4.18-4.94GHz as well as phase noise of -109dBc/Hz at 1MHz from 4.5GHz carrier. The effective linear range has been extended by 38 percent.**

Index Terms — **voltage controlled oscillators, linear-range varactor.**

I. INTRODUCTION

In recent years, various fully integrated LC voltage controlled oscillators have been demonstrated [1]-[2]. Although most reports focus on achieving low phase noise, very few publications discuss the problem of a nonlinear VCO gain. When designing frequency synthesizers, a linear VCO gain is desirable so that PLL loop dynamics, such as settling time and phase margin, do not change with control voltage [3]. Generally, varactors are nonlinear and linear VCO gain over the whole control voltage range is difficult to achieve. Consequently, synthesizer designers often choose to operate the VCO over very narrow control voltage range where VCO gain is relatively linear [4]. In this project, only readily available tuning elements were MOS transistors. Unfortunately, MOS inversion capacitors are tunable over very narrow control voltage range. Hence, if MOS inversion capacitor is used as varactor, a method of linear range extension is desirable. This paper presents a 5GHz LC VCO using NMOS inversion varactors with extended linear tuning range. The implemented prototype has also a frequency divider and a low-dropout voltage regulator.

II. PROPOSED TECHNIQUE

A linearization technique, often used in Gm-C filters [5]-[6], based on the superposition of several offset nonlinear transfer characteristics can be used. Recently, this linearization technique has been applied to linearize VCO tuning characteristics by offsetting accumulation varactors [7]. Since MIM-capacitors and accumulation varactors are not available in this process, the technique presented in [7] cannot be used directly.

Figure 1 shows the conceptual diagram for two offset nonlinear capacitances C1, C2, and the composition C1+C2. In theory, a linear tuning range of the combined C1+C2 varactor can be effectively doubled as compared to individual varactors C1 and C2. An implementation of this concept is to combine MOS inversion varactors with different threshold voltages. In modern CMOS processes, MOS transistors with several threshold voltages are often available. Figure 1 also shows the simulated linear tuning range extension using normal threshold voltage (NV_T) and low threshold voltage (LV_T) transistors. The effectiveness of this approach is shown in Figure 2 where VCO tuning curves with NV_T+NV_T and NV_T+LV_T varactor combinations are compared. The NV_T+NV_T varactors based VCO shows a linear range of 360mV, whereas the NV_T+LV_T varactors based VCO shows a linear range of 500mV, which corresponds to a linear range extension of 38 percent. Since the offset mechanism is achieved with different MOS threshold voltages no auxiliary bias circuits are needed, and therefore, any potential phase noise degradation due to the bias noise is avoided [7]. Also, there is no penalty in the area and power consumption by using this proposed technique.

III. CIRCUIT DESIGN

A complete LC VCO based on NV_T+LV_T MOS-inversion varactor combination was designed and its schematic is shown in Figure 3. NV_T+LV_T MOS inversion varactors are used for fine tuning, and 5-bit binary-weighted NV_T MOS inversion varactors are used for coarse tuning. A 3-bit programmable resistor is used for post-fabrication current consumption and phase noise optimization. An NMOS VCO structure was chosen to achieve large tuning range. Inductor uses the standard thickness top metal (less than 1um), and all MOS inversion varactors are implemented in differential fashion to maximize the quality factor [8]. Other coarse tuning approaches based on switched MIM-capacitors [9]-[11] could not be used because MIM-capacitors were not available in this process. Since gates of NMOS-varactors are connected directly to the supply voltage, the VCO

supply voltage needs to be regulated in order to minimize supply pushing.

This VCO circuit was designed into a test chip as shown in Figure 4. To accommodate frequency limitations of our measurement equipment, the VCO circuit was followed by a conventional CML divider [12], and a 50 ohm measurement buffer. A conventional low dropout voltage regulator [13]-[14] was included in the design to provide 1.5V regulated supply for high-speed circuits and to accommodate external supply voltages of 2.7V to 3.6V. To avoid VCO phase noise degradation from the regulator noise, a noise filter has been implemented using an on-chip resistor R_{nf} and an external capacitor C_{extnf} for the bandgap.

IV. MEASUREMENT RESULTS

The VCO, divider, buffer, and voltage regulator circuits have been implemented in a test chip fabricated in purely digital 0.15um CMOS process. During writing of this paper chip photo is not available, but the layout is shown in Figure 5. The chip has been packaged in QFN48 package and was mounted on a conventional FR4 evaluation board. All measurements were done using Agilent 4352B VCO/PLL analyzer.

Figure 6 shows the measured tuning characteristics for all 32 bands after divide-by-2. The measured tuning range after divide-by-2 extends from 2.09GHz to 2.47GHz, which corresponds to a VCO tuning range of 4.18GHz to 4.94GHz. Although larger band-to-band frequency step is visible between band 15 and 16, sufficient overlap exists to cover all frequencies.

The measured VCO gain after the divider is shown in Figure 7. The peak VCO gain after divide-by-2 varies from 41MHz/V to 63MHz/V for bands 0 to 31, respectively, which corresponds to 82MHz/V and 126MHz/V at the VCO output. The linear range where VCO gain is above 50% of the peak VCO gain is approximately 0.5V, which demonstrates the effectiveness of the proposed linear range extension technique.

Figure 8 shows the measured temperature drift of the VCO after divide-by-2. The measured temperature drift is 69MHz/135C and 85MHz/135C for bands 0 and 31, respectively. As can be seen, the temperature drift for this VCO is larger than frequency coverage of one single tuning curve, and this is a problem for frequency synthesizers that must operate continuously. In this case, a temperature drift compensation circuit must be added or alternatively VCO gain must be increased to cover temperature drift variation. However, in TDMA-type systems, since the frequency synthesizer regularly performs auto-band calibration, temperature drift is not a severe problem. We believe that the root cause of the large temperature drift is the temperature dependence of the inductor quality factor (i.e. temperature coefficient of the resistance due to aluminum metal traces). In this process, the measured inductor quality factors were from 2.7 to 3.3.

The measured supply pushing at the divide-by-2 output is shown in Figure 9. The worst case supply pushing for a 2.7V-3V supply variation is 150kHz, which corresponds to 300kHz/0.3V at the VCO output.

The measured phase noise after divide-by-2 is shown in Figure 10. The phase noise is -91dBc/Hz at 100kHz offset and -115dBc/Hz at 1MHz offset from 2.3GHz carrier. At 4.5GHz output this corresponds to a phase noise of -85dBc/Hz at 100kHz offset and -109dBc/Hz at 1MHz offset from the carrier.

The VCO and divide-by-2 circuit consume 4mA and 1.9mA of current from the regulated 1.5V supply.

V. CONCLUSION

A technique for extending the linear tuning range of a VCO has been presented. The technique is suitable for VCO implementations in purely digital processes where MIM-capacitors are not present and only MOS transistors are available. The proposed technique has been demonstrated in a 0.15um CMOS test chip with a 5GHz LC VCO, including divide-by-2 and internal low-noise voltage regulator circuits.

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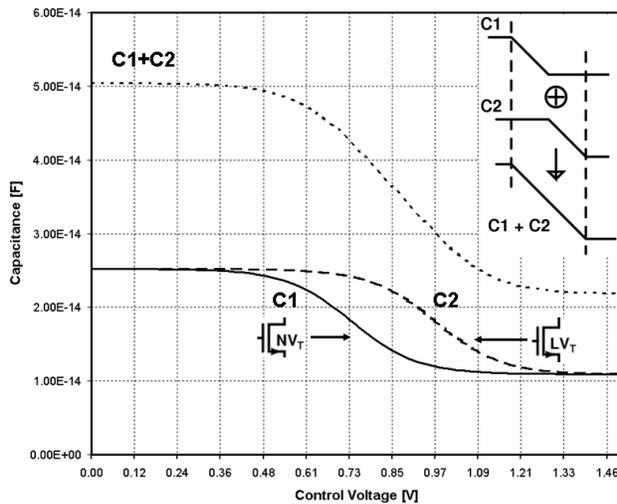
Figure 1: Concept and range extension simulated data for low & regular threshold MOS-capacitors.
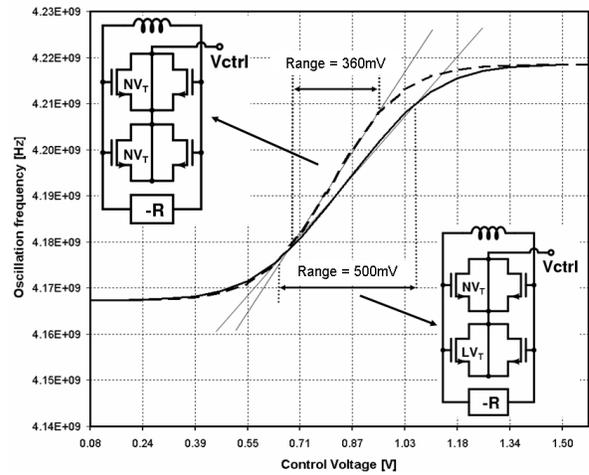

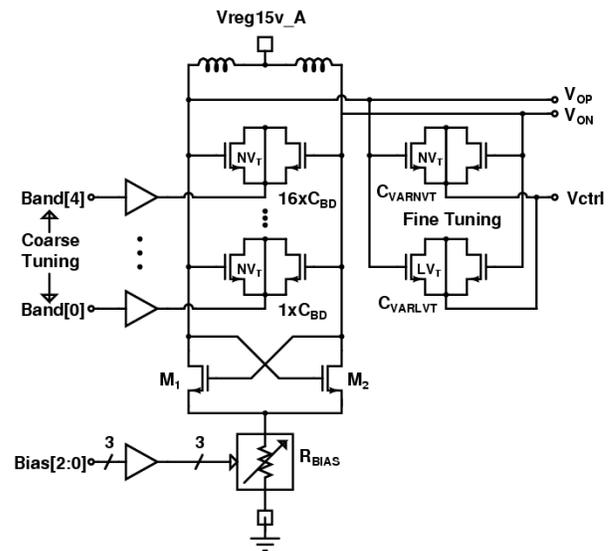Figure 2: Simulated range extension for a VCO circuit.

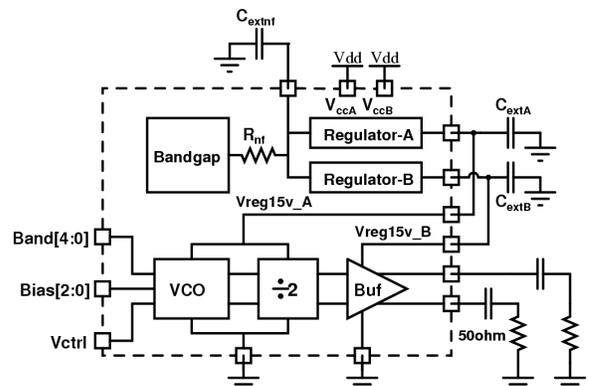Figure 3: VCO using extended linear-range varactor.

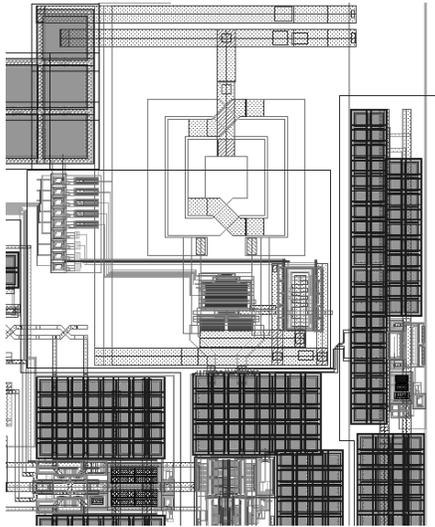

Figure 4: Block diagram of the VCO test chip.

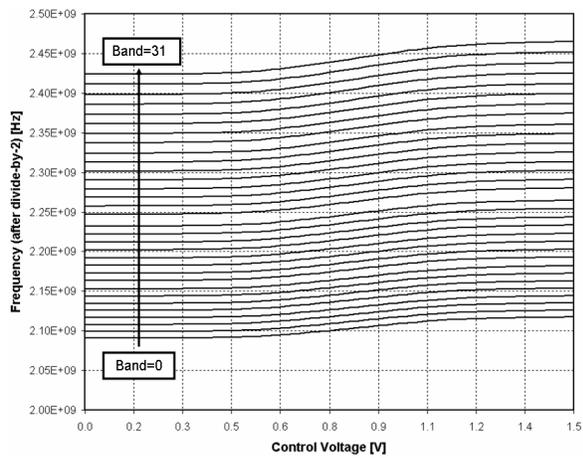Figure 5: Layout diagram of the proposed VCO.

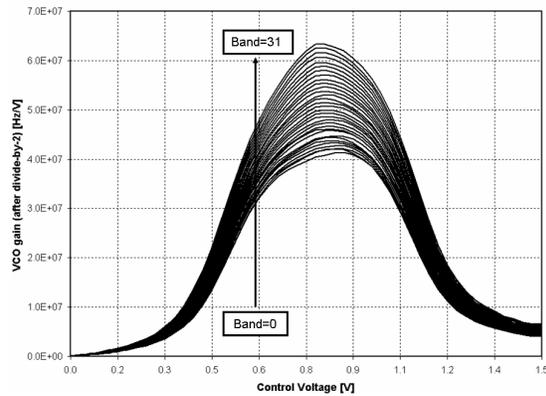Figure 6: Measured frequency tuning (after div/2).

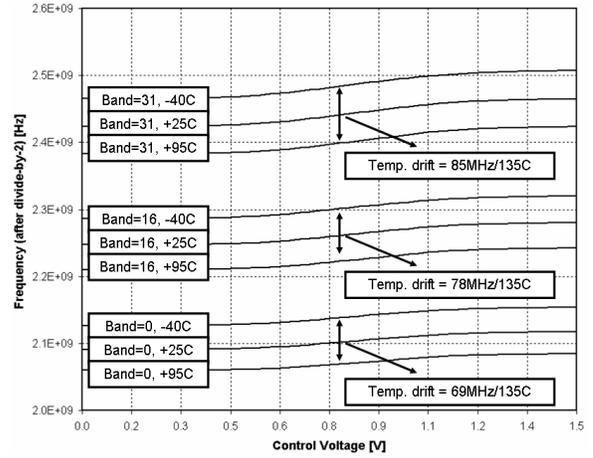

Figure 7: Measured VCO gain (after div/2).

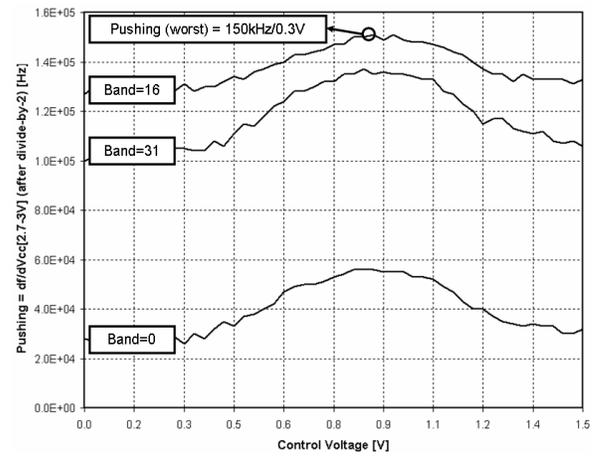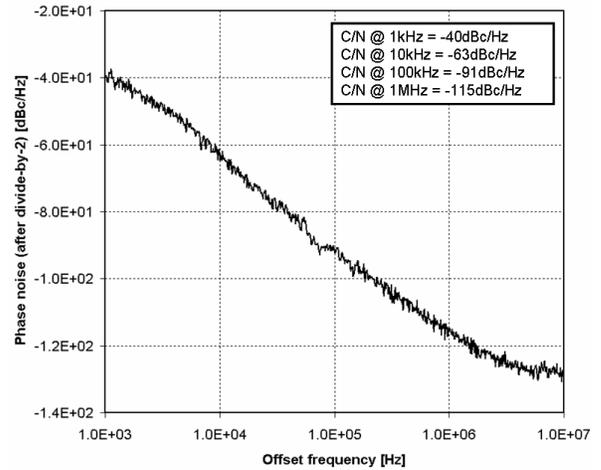Figure 8: Measured temperature drift (after div/2).

Figure 9: Measured supply pushing (after div/2).

Figure 10: Measured phase noise (after div/2).