A Widlar-Bandgap based Intermediate-Frequency Voltage-Controlled Oscillator for GSM/DCS Transceiver ICs

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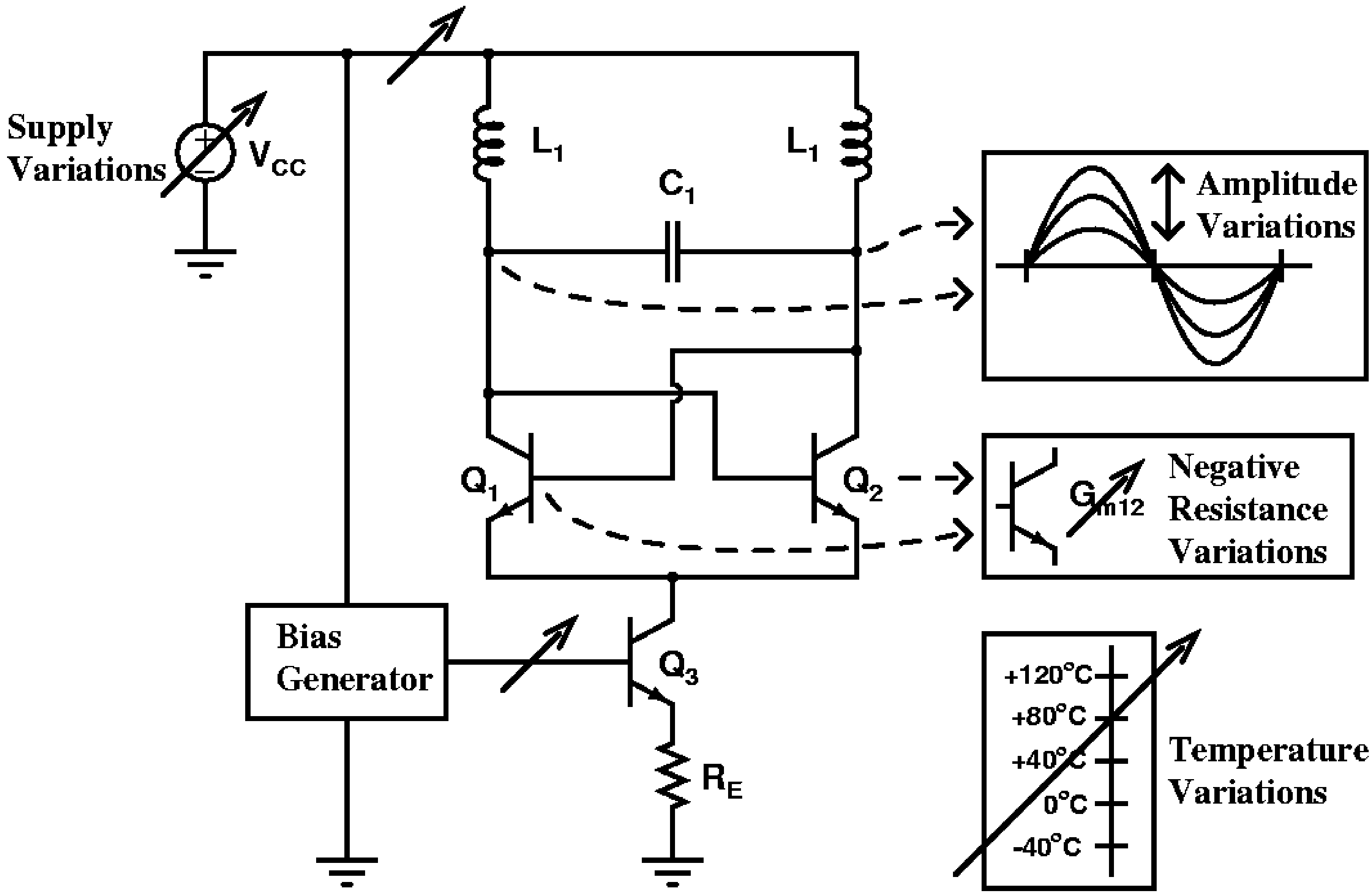
2003 IEEE RFIC Symposium, Philadelphia, PA, June 10, 2003
Paper: IFTU-80

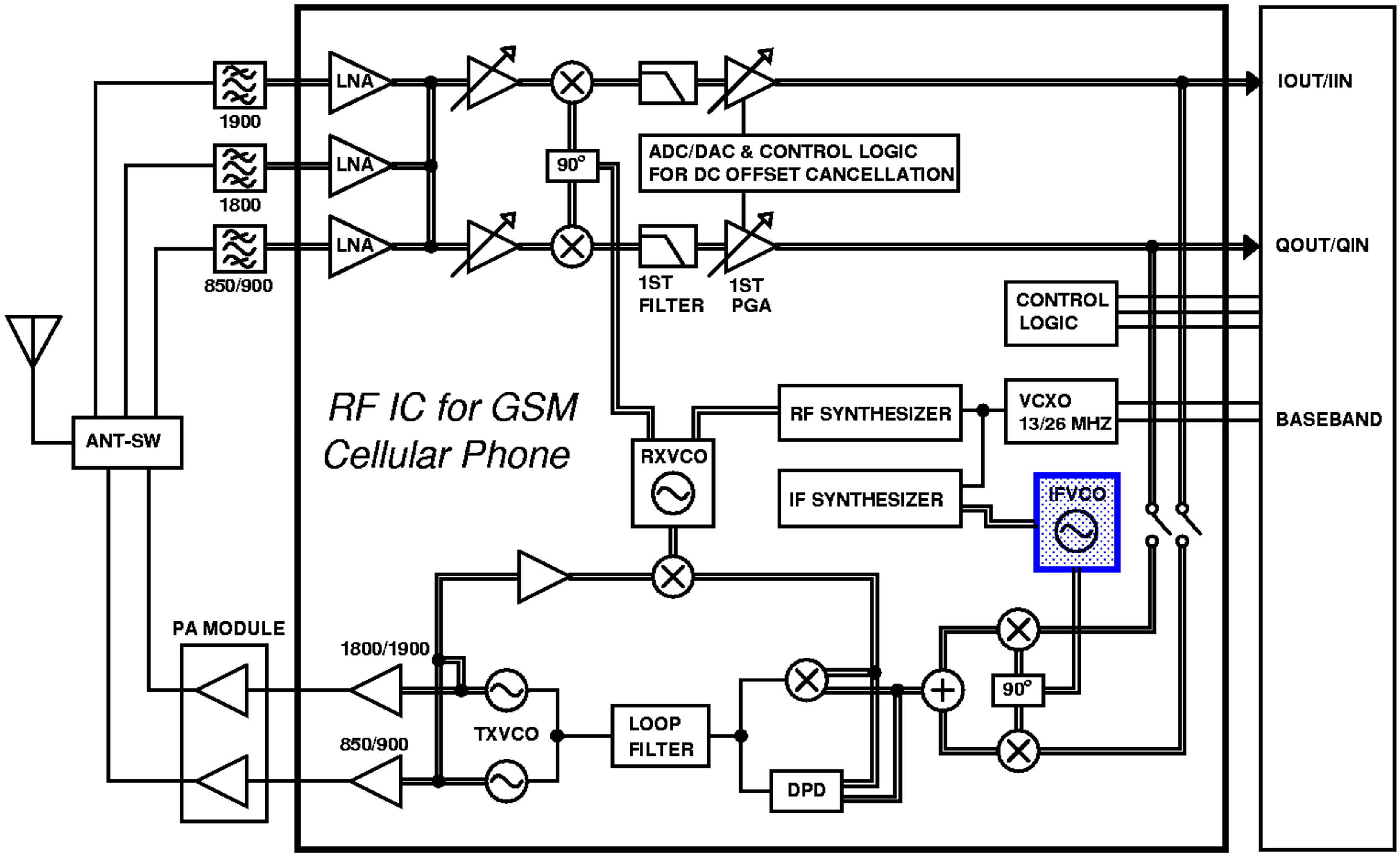
Outline

- Introduction
- Application: RF IC for GSM cellular phone
- Approaches for supply and temperature insensitive VCO:
  - Conventional approach: using bandgap-referenced VCO bias current
  - Embedded approach: VCO embedded in Widlar-bandgap
- Simulation results
- Experimental results
- Summary
- Acknowledgements

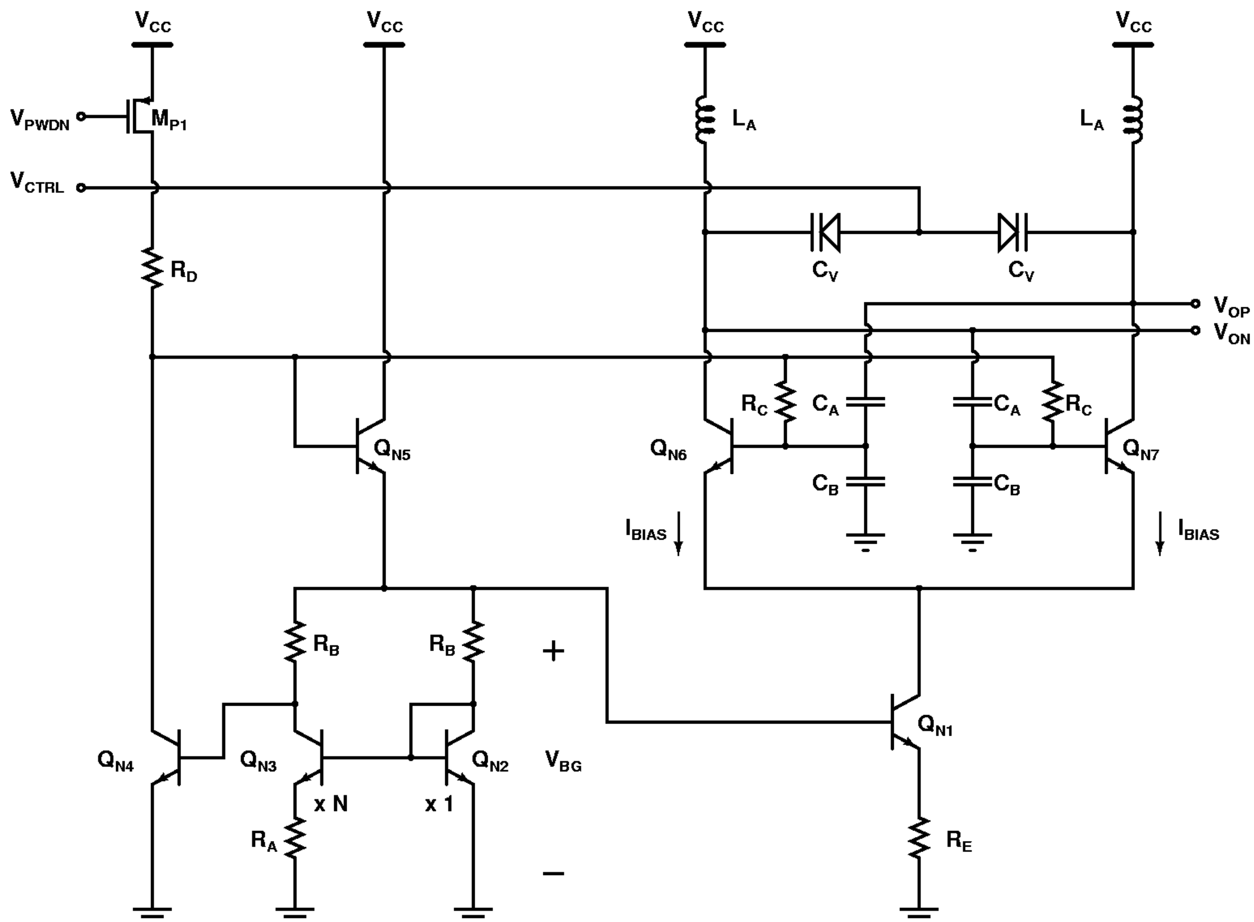
Introduction



Application: RF IC for GSM Cellular Phone



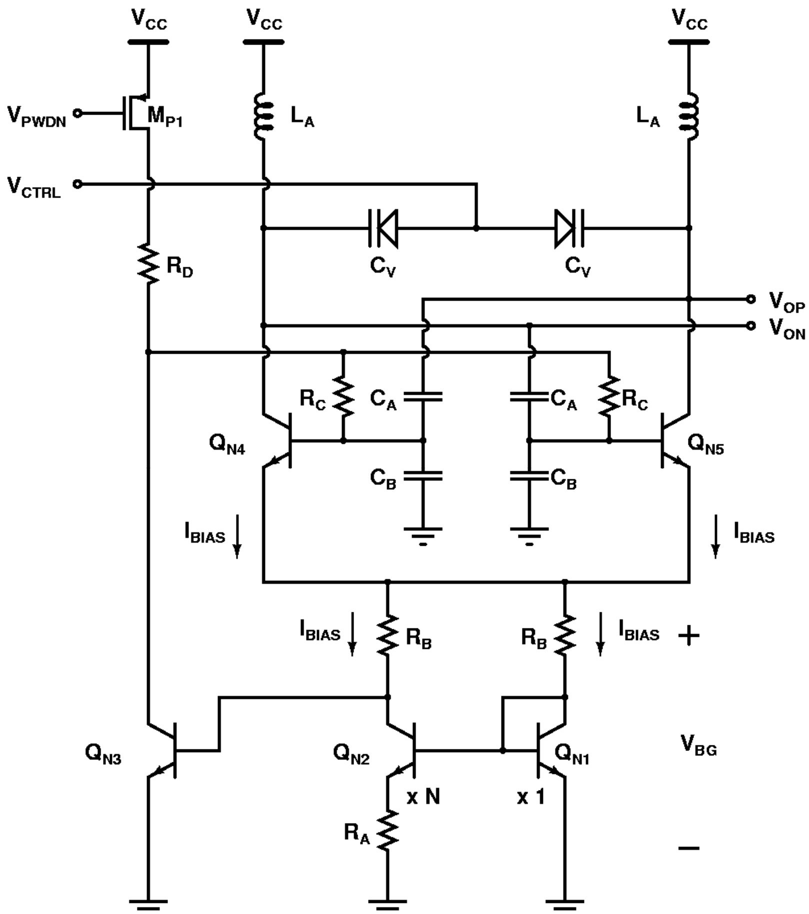
Conventional Approach for DC-Bias of VCO



Bandgap reference (Widlar bandgap)

VCO with supply insensitive DC-bias & temperature insensitive loop gain

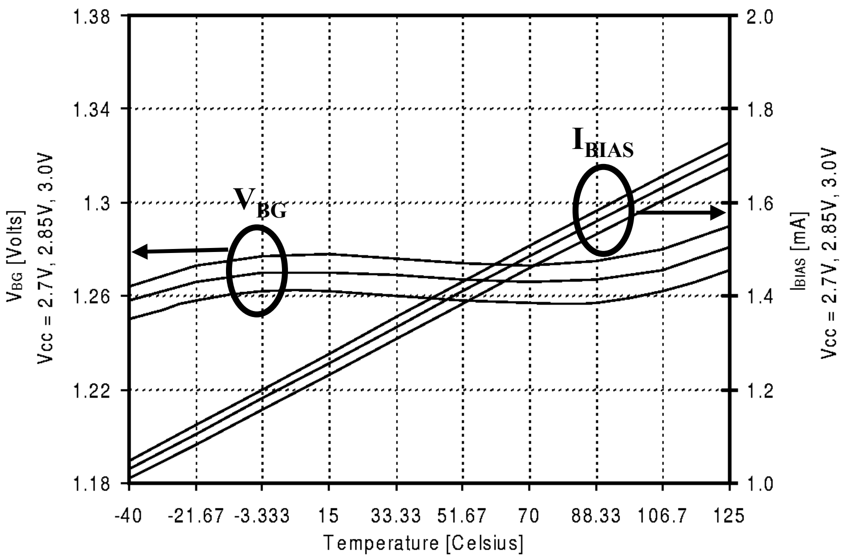
Embedded Approach for DC-Bias of VCO



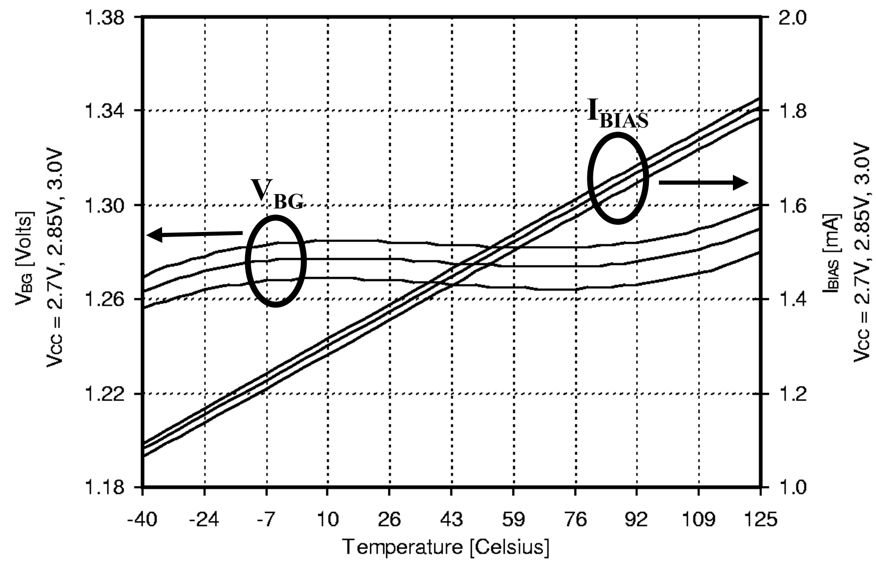
VCO embedded in Widlar-Bandgap for supply insensitive DC-bias & temperature insensitive loop gain - eliminated devices for low power and less noise

Simulated DC Operating Point Characteristics (SpectreRF)

Conventional Approach



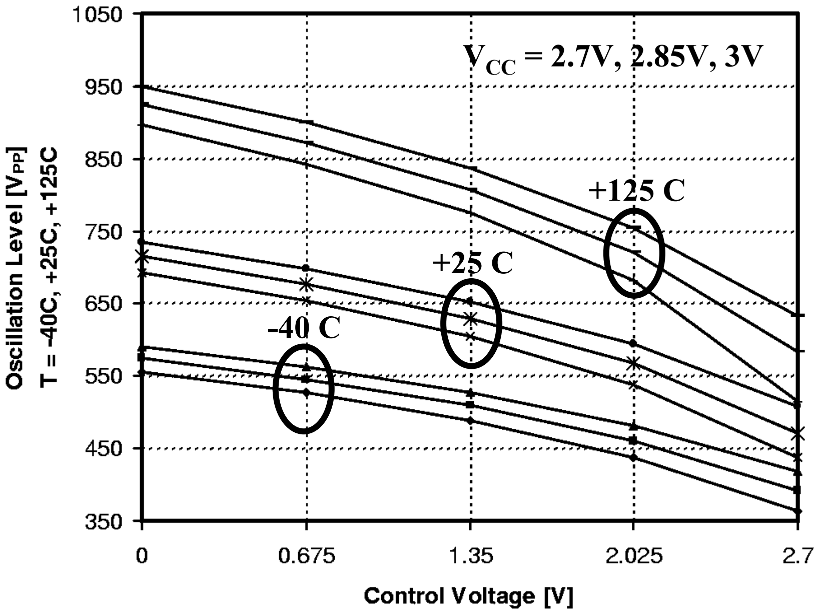
Embedded Approach



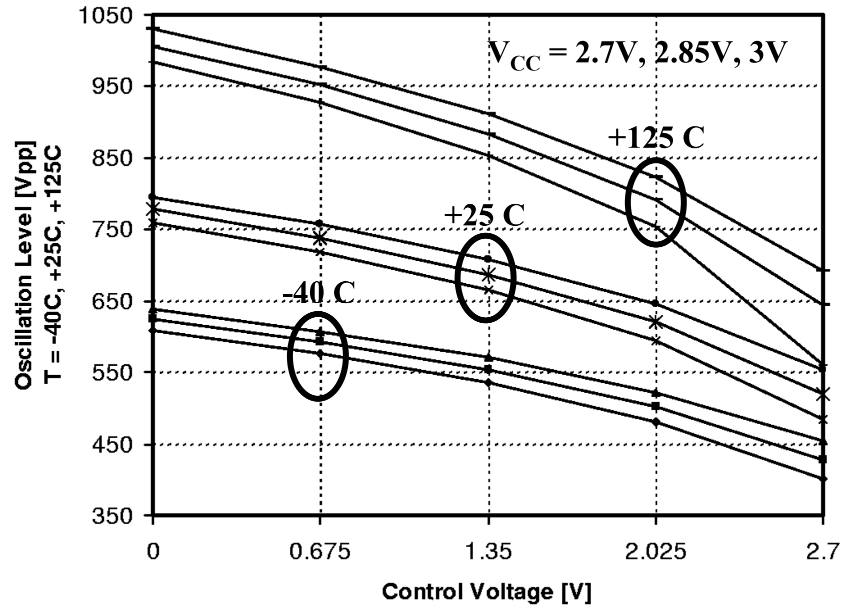
Embedded approach achieves same DC-bias behavior as conventional approach (PTAT bias current → g_m of VCO NPN's constant over temperature)

Simulated VCO Steady State Characteristics (SpectreRF)

Conventional Approach



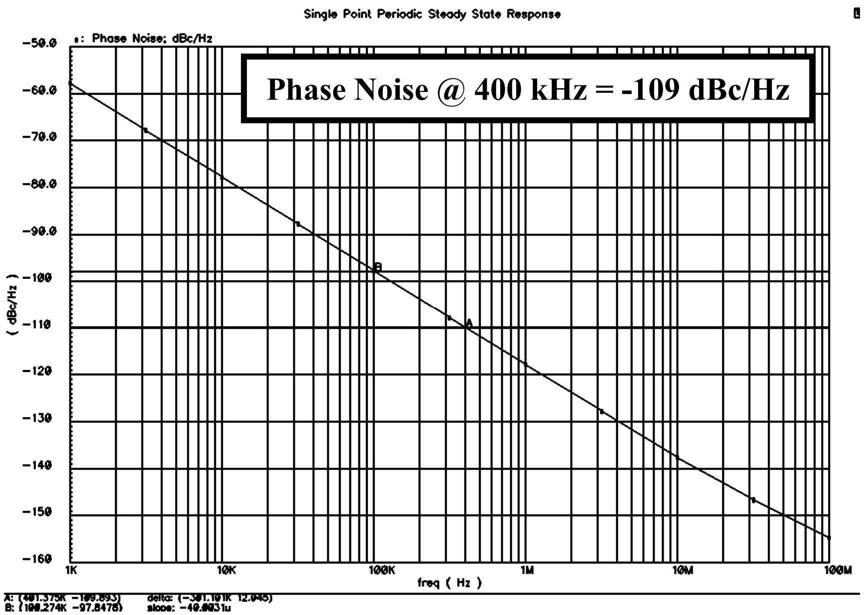
Embedded Approach



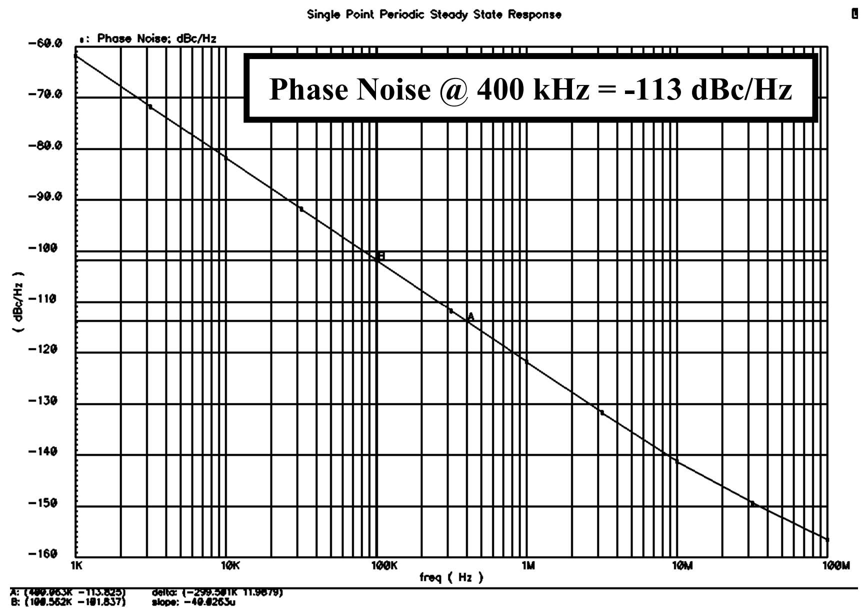
Embedded approach achieves the same VCO steady-state characteristics as conventional approach (oscillation amplitude increases with temperature)
Small variation in oscillation amplitude over supply variation

Simulated VCO Phase Noise Characteristics (SpectreRF)

Conventional Approach

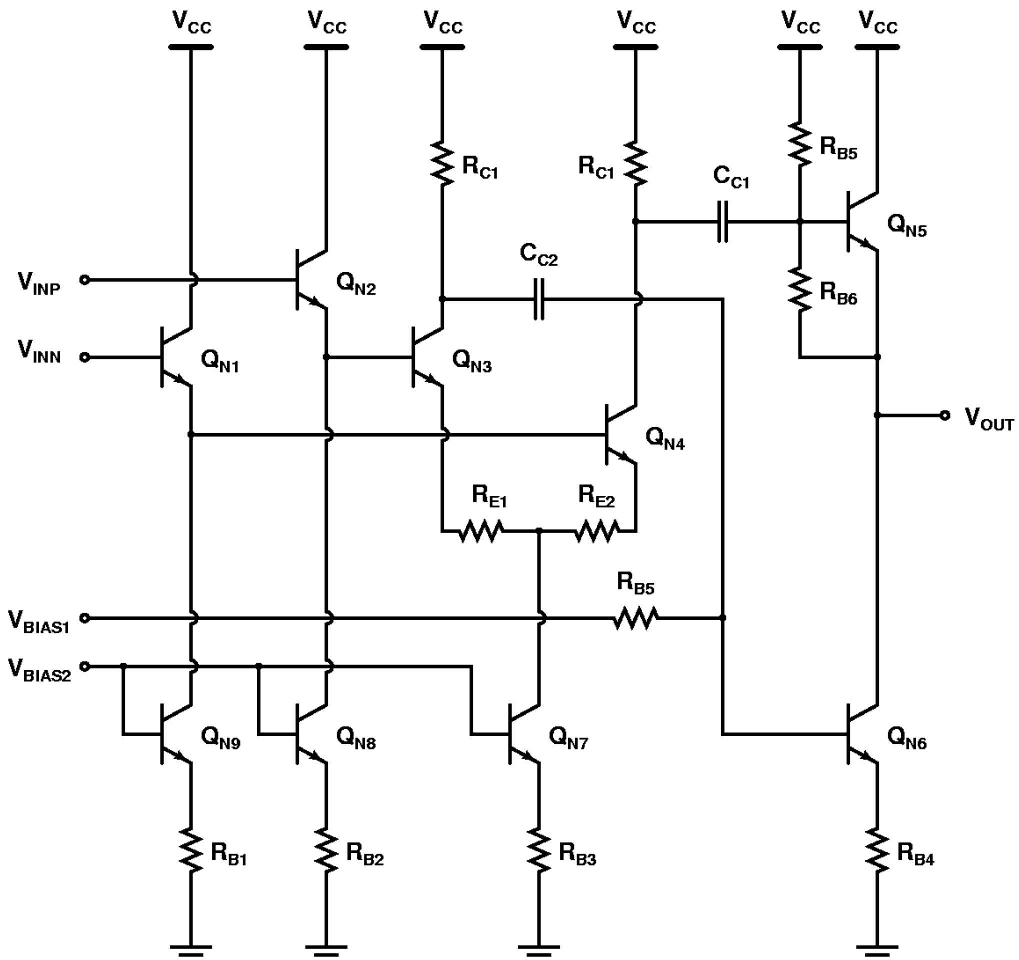


Embedded Approach



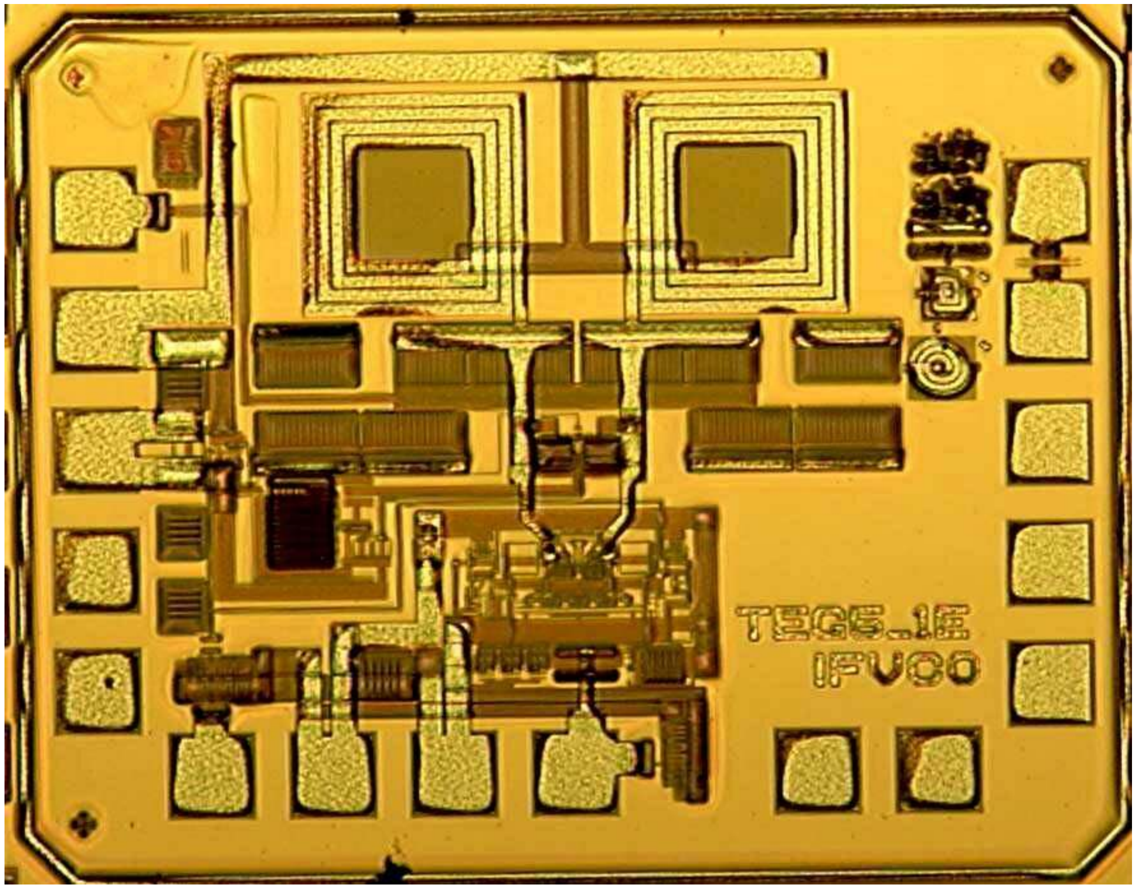
Embedded approach achieves 4 dB better phase noise over conventional approach (same VCO voltage-swing & power consumption in VCO-core)

Output Buffer Schematic



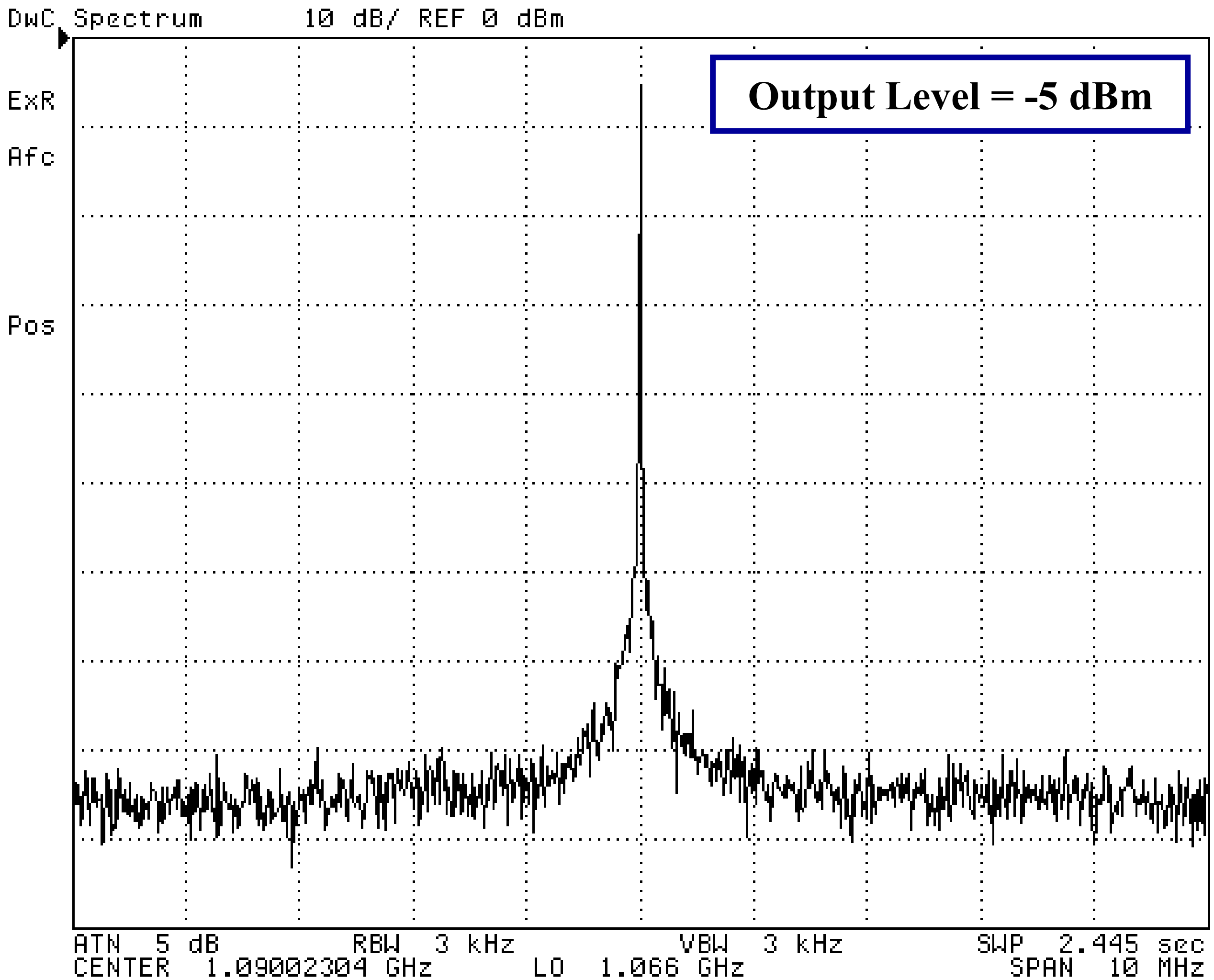
Bipolar output buffer for driving the 50 Ohm measurement equipment

Chip Microphotograph

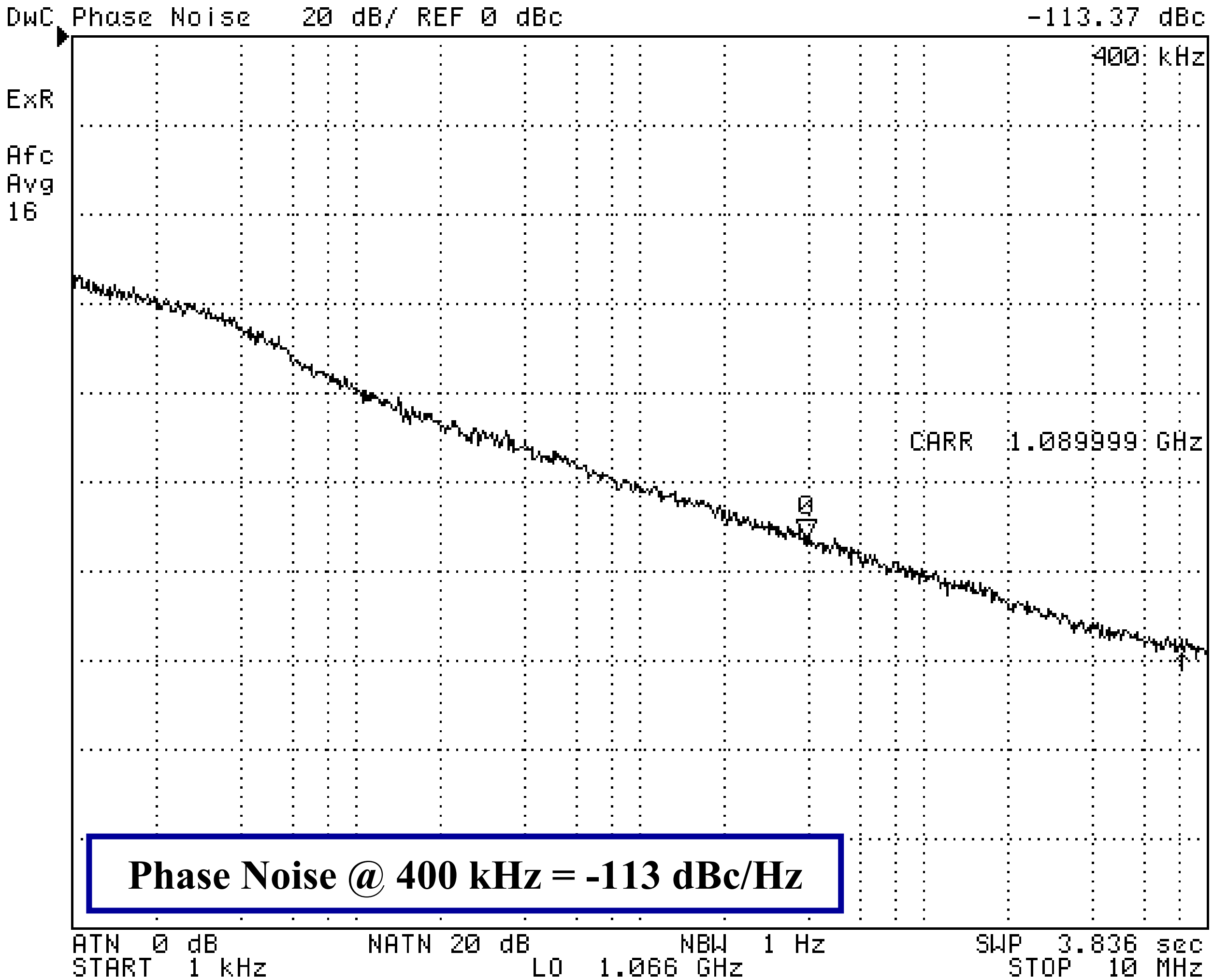


Embedded approach: 1 GHz IF-VCO in 0.35 μm SOI BiCMOS
(Chip size: 1.5mm X 1.2 mm)

Measured Output Spectrum

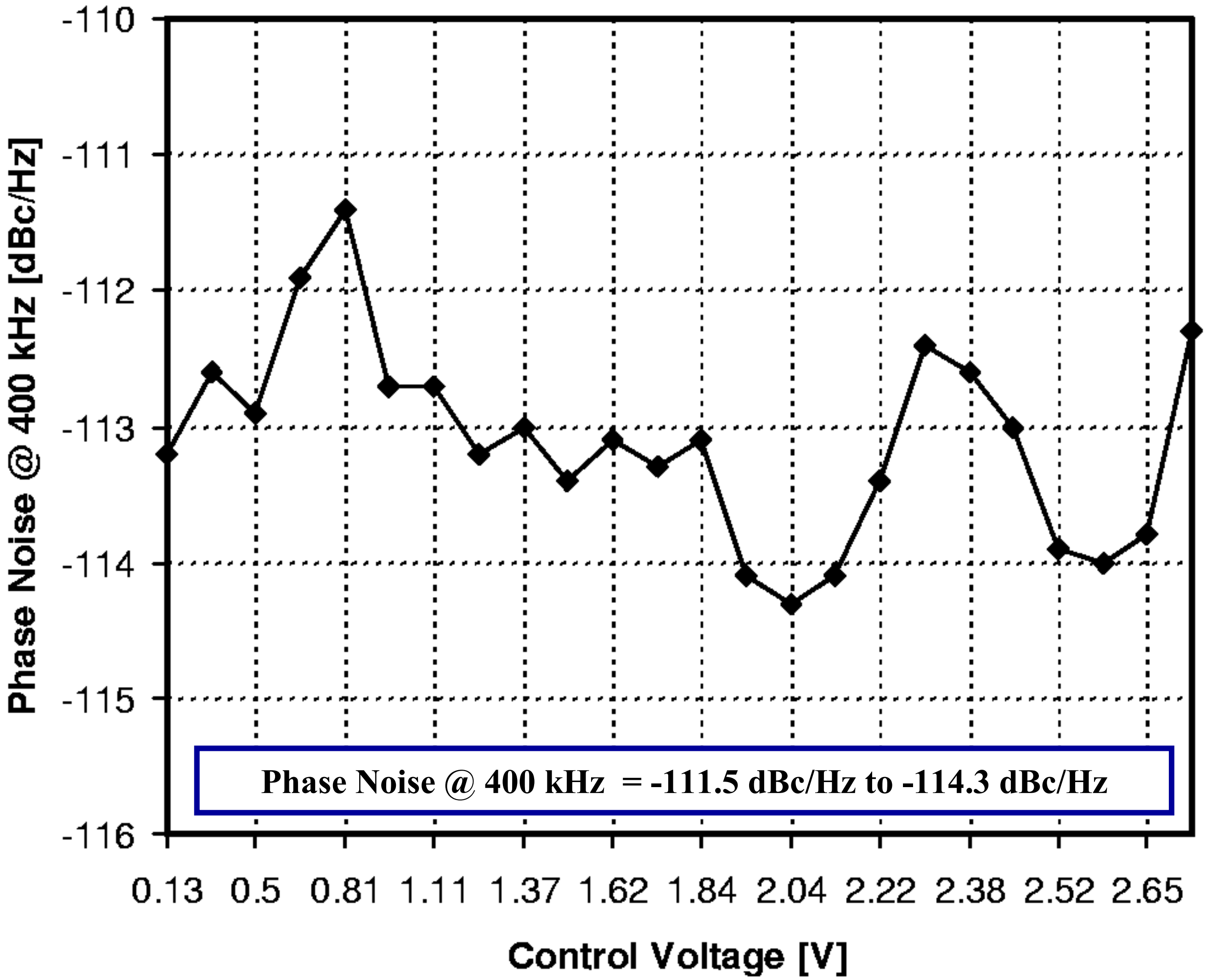


Measured Phase Noise

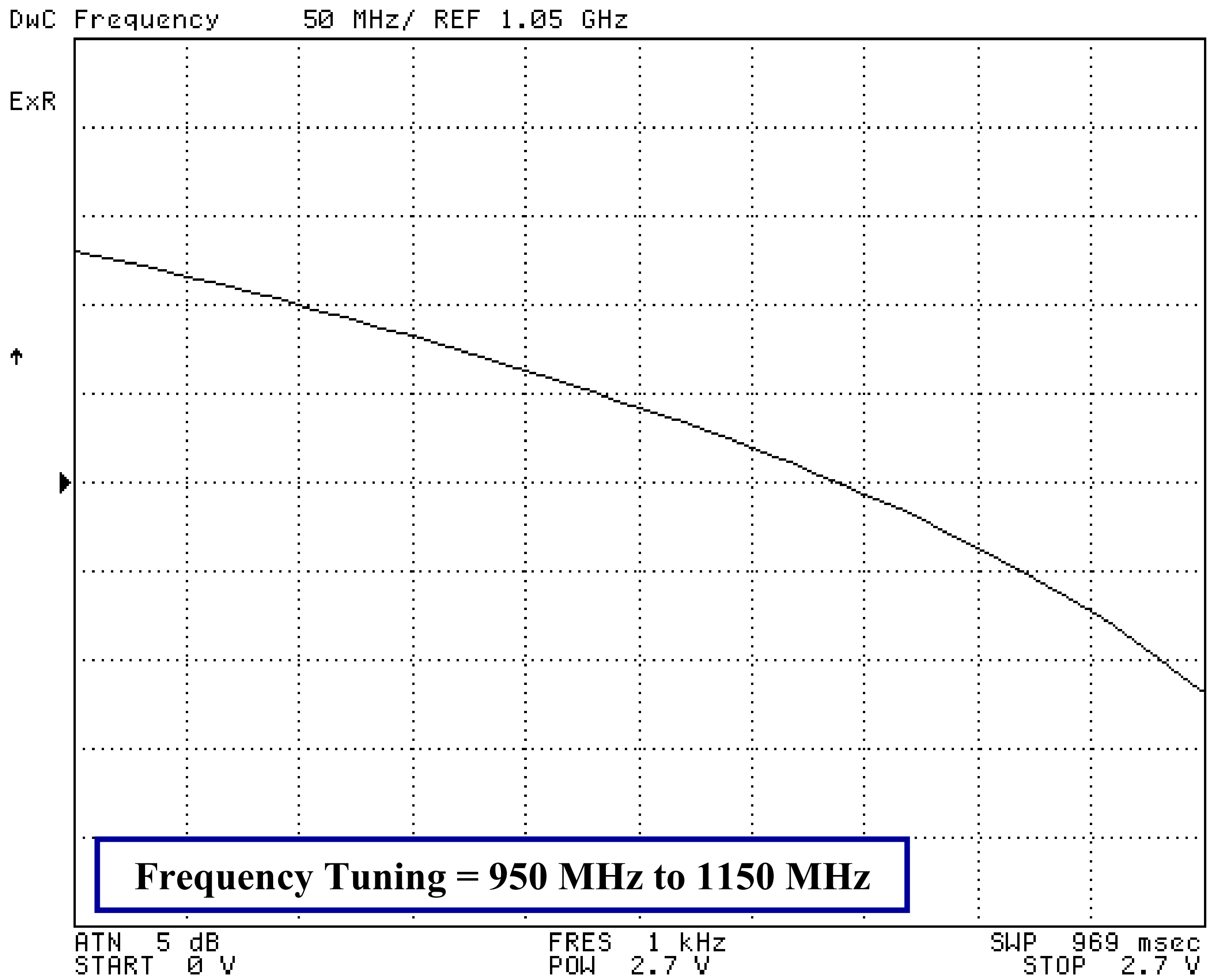


Phase Noise @ 400 kHz = -113 dBc/Hz

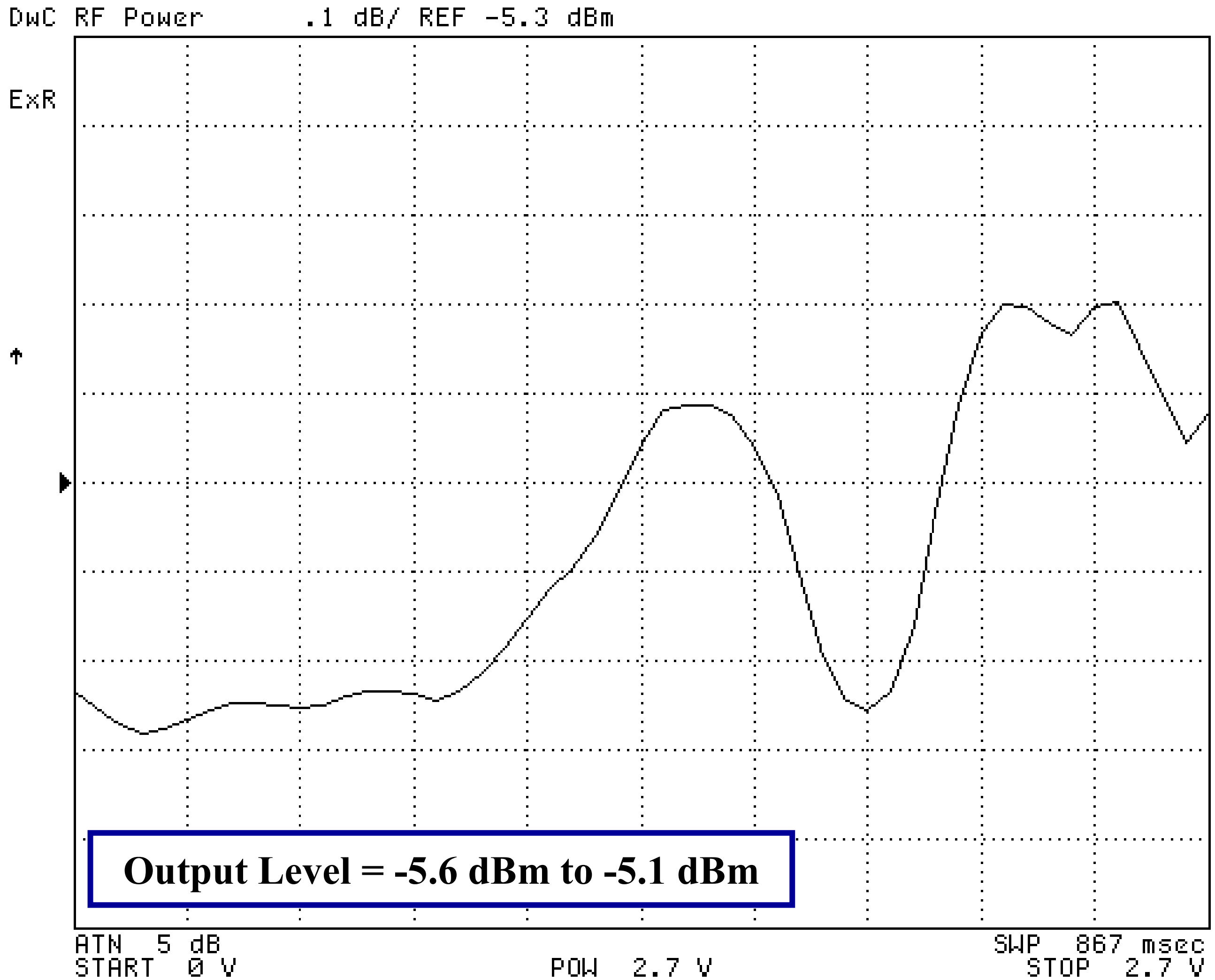
Measured Phase Noise Control-Voltage Characteristics



Measured Frequency Tuning Characteristics



Measured Output Level Characteristics



Summary

Characteristics	*1 GHz VCO*	*500 MHz VCO*
Technology	0.35 μm SOI BiCMOS	0.35 μm SOI BiCMOS
Supply Voltage [Volts]	2.7	2.7
VCO Supply Current [mA]	4	4
Buffer Supply Current [mA]	11	11
Output Level [dBm]	-5.1	-3.4
Frequency Tuning [MHz]	931 - 1180	415 - 543
Phase Noise @ 100 kHz [dBc/Hz]	-102	-103
Phase Noise @ 400 kHz [dBc/Hz]	-113	-114

Conclusion

- Conventional VCO DC-bias approach
  - Supply variation insensitive DC-bias & oscillation amplitude
  - Temperature variation insensitive negative resistance
- Embedded VCO DC-bias approach
  - Same DC-bias & steady-state characteristics over supply & temperature as the conventional approach
  - Lower power and smaller chip area (due to eliminated devices)
  - Phase noise 4 dB better than conventional approach
- Embedded approached demonstrated in 1 GHz IF-VCO, implemented in 0.35 μm SOI BiCMOS