A Widlar-Bandgap based Intermediate-Frequency Voltage-Controlled Oscillator for GSM/DCS Transceiver ICs

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***Abstract* — This paper presents an intermediate-frequency voltage-controlled oscillator using a Widlar-Bandgap for stable operation over supply and temperature variations without degrading the phase noise performance. The design is fabricated in a 0.35 μm SOI BiCMOS and is packaged in a QFN24 plastic package. The VCO operates at 1 GHz with a tuning range of 250 MHz and achieves a phase noise of –113 dBc/Hz at 400 kHz offset from the carrier. The VCO core and buffer consume 4 mA and 11 mA from a 2.7 V power supply, respectively. The IF-VCO is suitable for GSM/DCS transceiver IC applications.**

I. INTRODUCTION

Recent advances in integrated circuit (IC) technologies have facilitated the realization of single chip transceivers for even such applications as the GSM cellular telephone standard [1],[2]. Voltage controlled oscillators (VCOs), however, are some of the most difficult components to integrate on-chip due to stringent system specifications [1],[2]. System specifications often require VCOs with very low phase noise while minimizing power and chip area. Since the phase noise of a VCO is inversely proportional to the quality factor (Q-factor) of the LC-tank, high-Q passive components such as inductors, capacitors, and varactors are needed to realize low phase noise VCOs [3],[4]. High-Q passive elements are also needed to achieve low power consumption [3],[4]. Thus, in order to make integrated VCOs and other RF building blocks possible, today's advanced technologies often offer not only high-frequency bipolar and MOS transistors but also high-Q passive elements such as inductors, capacitors, and varactors [1],[2]. High-Q inductors are othen realized using thick metal [1],[2],[5], while high-Q varactors are often implemented using proper layout techniques [6].

Many VCOs in both bipolar (for example, [7], [8]) and CMOS technologies (e. g. [9]-[10]) have been reported. However, little attention has been paid to VCO bias techniques for achieving low phase noise while maintaining stable operating point over supply and temperature variations. In this paper, a Widlar Bandgap is embedded into an intermediate-frequency voltage-controlled oscillator (IF-VCO) for stable DC-bias over supply and temperature variations.

II. VCO DESIGN

The schematic of the IF-VCO is shown in Fig. 1. The negative resistance of the VCO is realized using differential pair transistors Q_{N4}-Q_{N5} as well as coupling capacitors C_A-C_B. These coupling capacitors are chosen to attenuate the signal at the base of transistors Q_{N4}-Q_{N5} to allow sufficient voltage swing at the collector without transistors entering the saturation region. The LC-tank consists of spiral inductors L_A and *PN*-junction varactors C_V. Bias resistors R_C are chosen sufficiently large so that they do not disturb the Q-factor of the LC-tank.

A stable DC operating point over supply and temperature variations is obtained by embedding the VCO in a Widlar bandgap [11]. The Widlar bandgap consists of transistors Q_{N1}-Q_{N5} where transistor Q_{N3} ensures that the collector voltage of Q_{N2} is equal to V_{BE}. Since both collector voltages of transistors Q_{N1}- Q_{N2} are at V_{BE}, the bias current I_{BIAS} flowing through the resistors R_B is the same. Furthermore, because transistor Q_{N2} is N times larger than Q_{N1} transistor, a bias current I_{BIAS} that is proportional to absolute temperature (PTAT) is achieved [11]. With a PTAT bias current I_{BIAS}, the transconductance of VCO transistors Q_{N4}-Q_{N5} is independent of temperature and insensitive to supply voltage variations [12].

The IF-VCO with an oscillation frequency of 1 GHz has been designed by selecting a 5.3 nH inductance for the spiral and a 2.5 pF to 5.0 pF variable capacitance for the *PN*-junction varactor. ASITIC was used to model the spiral inductor [13]. The inductor is 320 μm on a side and uses 15 μm wide track width to reduce resistance. The inductance is realized using 5 turns with 3 μm spacing. Isolation mesh is implemented underneath the inductor to minimize possible eddy currents. The IF-VCO design has been simulated using the Spectre/SpectreRF simulator from Cadence. Fig. 2 shows the simulated DC-operating point of the VCO over supply and temperature variations.

The emitter voltage of transistors Q_{N4}-Q_{N5} has a simulated DC-bias variation of approximately 44 mV over 2.7 V to 3.0 V supply and –40 C to 125 C temperature variation. The bias current I_{BIAS} is proportional to absolute temperature and exhibits a simulated bias current variation of approximately 40 μA over 2.7 V to 3.0 V supply variation. The VCO consumes 3.1 mA from a 2.7 V power supply at 25 C. The simulated tuning range of the VCO is 246 MHz, while the oscillation level of the VCO varries from 530 mV_{PP} to 790 mV_{PP} over control voltage range of 0 V to 2.7 V. Over supply voltage variation of 2.7V to 3.0V the oscillation level varies by approximately 60 mV. The oscillation level increases with temperature, since bias current of the VCO core transistors is proportional to absolute temperature. At 125 C, the oscillation level is approximately 1.6 times the oscillation level at –40 C over entire control voltage range. The simulated phase noise of the VCO is –101.8 dBc/Hz and –113.8 dBc/Hz at 100 kHz and 400 kHz offsets from the carrier, respectively. According to SpectreRF, the largest contribution of noise to VCO phase noise at 100 kHz and 1 MHz offsets from the carrier comes from transistors Q_{N4}-Q_{N5} (approximately 50 %) and loss in spiral inductors (approximately 21 %). Embedding the VCO inside the Widlar-bandgap as shown in Fig. 1 does not have significant adverse effects on phase noise, which is one of the advantages of this circuit topology.

II. BUFFER DESIGN

Fig. 3 shows the schematic of the output buffer that is used to drive the 50 Ω measurement equipment. The output of the VCO is DC-coupled using emitter followers composing of transistors Q_{N1}-Q_{N2}. The emitter followers buffer the signal as well as provide the voltage shifting needed to properly bias the differential pair transistors Q_{N3}-Q_{N4}. Degeneration resistors Q_{N3}-Q_{N4} are used to reduce the magnitude of the harmonics. The output of the differential pair is coupled to the output transistors Q_{N5}-Q_{N6} using capacitors C_{C1}-C_{C2}. Resistors R_{B5}-R_{B6} are used to bias the output of the buffer to 1.5 V_{BE} below supply voltage. The output stage operates in a class AB mode, and using an external bypass capacitor, the output stage drives directly the 50 Ω load. The buffer design was simulated using the Spectre/SpectreRF simulator. The buffer draws a simulated current of 10.2 mA from a 2.7 V power supply at 25 C. The output buffer harmonics are –18.7 dBc below the carrier, while the output buffer delivers a power of –3.6 dBm into 50 Ohm load.

III. EXPERIMENTAL DESIGN

The IF-VCO was fabricated in a 0.35 μm BiCMOS technology [14], which has 4 layers of aluminum. The process features 2 μm top aluminum layer, which makes possible integration high-Q spiral inductors. High-density metal-insulator-metal (MIM) capacitors as well as a zero temperature coefficient polysilicon resistor are also available in this process. The passive devices used in the VCO have been characterized on wafer. The 2.5 pF to 5.0 pF *PN*-junction varactor has a measured Q-factor of 63 at 1 GHz, while the 5.3 nH spiral inductor has a measured Q-factor of 6.5 at 1 GHz.

Microphotograph of the IF-VCO is shown in Fig. 4. The die was packaged in a QFN24 plastic package. Fig. 5 shows the measurement setup. The packaged device was assembled on a FR-4 PCB board and all measurements were performed using an Agilent 4352B VCO/PLL analyzer.

For phase noise and output spectrum measurements, the oscillation frequency of the IF-VCO was set to 1.09 GHz using a low phase noise frequency reference and an internal narrowband PLL of the 4352B analyzer. Fig. 6 shows the measured output spectrum where the output level of the VCO is – 5.1 dBm. The second harmonic and third harmonics are –26 dBc and –15 dBc below the fundamental. Fig. 7 shows the measured phase noise. At 100 kHz offset from the 1.09 GHz carrier, the measured phase noise is –102 dBc/Hz, while at 400 kHz offset from the carrier the phase noise is –113 dBc/Hz. Tuning characteristics of the VCO are shown in Fig 8. For a control voltage change of 0 V to 2.7 V, the VCO tunes from 931 MHz to 1181 MHz. From a 2.7V power supply, the VCO and output buffer consume 4 mA and 11 mA, respectively.

In addition to the 1 GHz IF-VCO, a 500 MHz IF-VCO was also fabricated. The 500 MHz VCO has a tuning range of 128 MHz, and a phase noise of –103 dBc/Hz and –114 dBc/Hz at 100 kHz and 400 kHz offsets from the carrier, respectively. The measurement results for 1 GHz and 500 MHz IF-VCOs are summarized in Fig. 9.

IV. CONCLUSION

A novel VCO circuit based on Widlar-bandgap which does not have adverse effects on phase noise has been presented. IF-VCOs operating at 1 GHz and 500 MHz have been demonstrated. Measurement results compare well with simulations. These IF-VCOs are suitable for GSM/DCS transceiver applications [15].

ACKNOWLEDGEMENT

The authors wish to acknowledge the assistance and support of Masao Hotta, Tomomitsu Kitamura, Yuichi Saito, Kentaro Suzuki, Satoshi Tanaka, and Kazuo Watanabe of Hitachi, Ltd.

REFERENCES

[1] A. Molnar, et. al., "A single-chip quad-band (850/900/1800/1900MHz) direct-conversion GSM/GPRS RF transceiver with integrated VCOs and fractional-N synthesizer," in *IEEE ISSCC Tech. Dig.*, Feb. 2002, pp. 232-233.

[2] S. Dow, et. al., "A dual-band direct-conversion/VLIF transceiver for 50GSM/GSM/DCS/PCS," in *IEEE ISSCC Tech. Dig.*, Feb. 2002, pp. 230-231.

[3] W. Robins, *Phase Noise in Signal Sources: Theory and Applications.* Stevenage, U.K.: Peregrinus, 1982, pp. 49-53.

[4] J. Craninckx, and M. Steyaert, "Low-noise voltage-controlled oscillators using enhanced LC-tanks," in *IEEE Trans. on Circuits and Systems-II*, vol. 42, no. 12, Dec. 1995, pp. 1474-1483.

[5] J. Burghartz, K. Jenkins, and M. Soyuer, "Multilevel-spiral inductors using VLSI interconnect technology," in *IEEE Electron Device Lett.,* vol. 17, Sep. 1996, pp. 428-430.

[6] A. Porret, T. Melly, C. Enz, and E. Vittoz, "Design of high-Q varactors for low-power wireless applications using standard CMOS process," in *IEEE J. of Solid-State Circuits*, vol. 35, no. 3, March 2000, pp. 337-345.

[7] M. Zannoth, B. Kolb, J. Fenk, and R. Weigel, "A fully integrated VCO at 2 GHz," in *IEEE ISSCC Tech. Dig.*, Feb. 1998, pp. 224-225.

[8] A. M. Niknejad, J. L. Tham, and R. G. Meyer, "Fully-integrated low phase noise bipolar differential VCOs at 2.9 and 4.4 GHz," in *Proc. of ESSIRC*, Sep. 1999, pp. 198-201.

[9] J. Craninckx, and M. Steyaert, "A 1.8 GHz low-phase-noise voltage-controlled oscillator with prescaler," in *IEEE J. of Solid-State Circuits*, vol. 30, no. 12, pp. 1474-1483.

[10] R. Aparicio, and A. Hajimiri, "A CMOS differential noise-shifting Colpitts VCO," in *IEEE ISSCC Tech. Dig.*, Feb. 2002, pp. 288-289.

[11] R. J. Widlar, "New developments in IC voltage regulators," in *IEEE Journal of Solid-State Circuits*, Vol. SC-6, pp. 2-7, Feb. 1971.

[12] W. Mack and R. Meyer, "A 1-GHz BiCMOS RF front-end IC," in *IEEE Journal of Solid-State Circuits*, Vol. SC-29, pp. 350-355, March 1994.

[13] A. Niknejad, "Modeling of passive elements with ASITIC," in *IEEE RFIC Symp. Dig.*, June 2002, pp. 303-306.

[14] T. Kikuchi, et. al., "A 0.35 um ECL-CMOS process technology on SOI for 1ns mega-bits SRAM's with 40ps gate array," IEDM, p. 923, Dec. 1995.

[15] S. Tanaka, et. al., "GSM/DCS1800 dual band direct conversion transceiver IC with DC calibration system," in *IEEE Proc. of ESSIRC*, Sep. 2001.

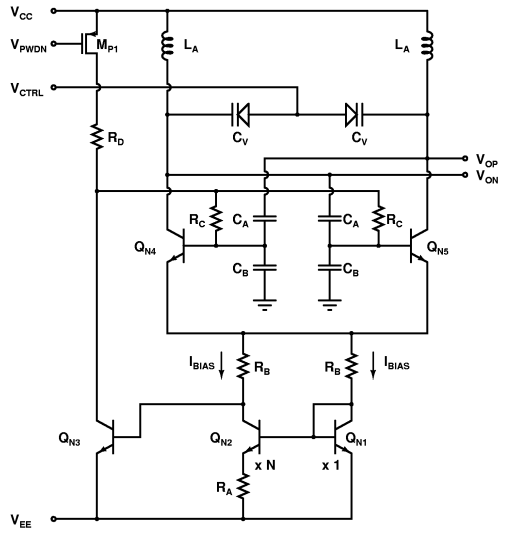

Fig. 1. VCO schematic (VCO embedded in Widlar-bandgap).

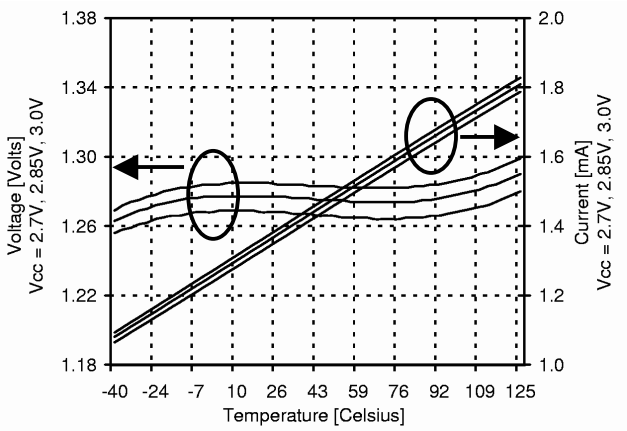

Fig. 2. Simulated DC-operating point of the VCO over supply and temperature variations (emitter voltage of Q_{N4}-Q_{N5} and bias current I_{BIAS}).

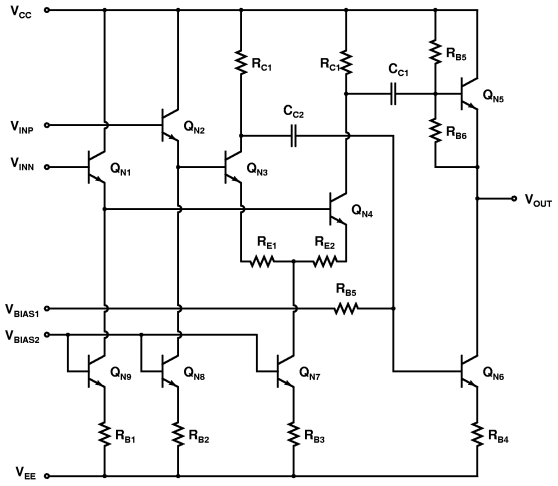

Fig. 3. Output buffer schematic.

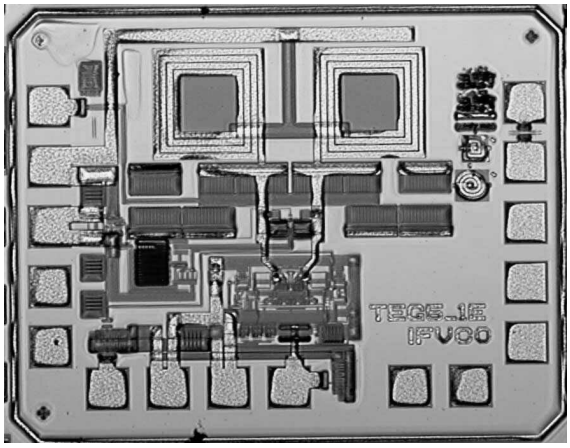

Fig. 4. Chip microphotograph.

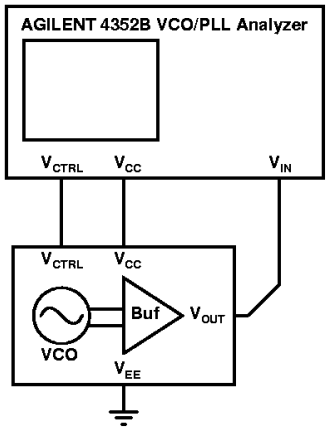

Fig. 5. Measurement setup.

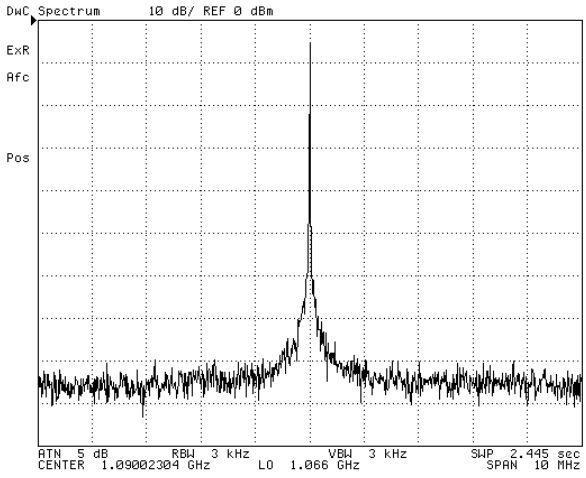

Fig. 6. Output spectrum.

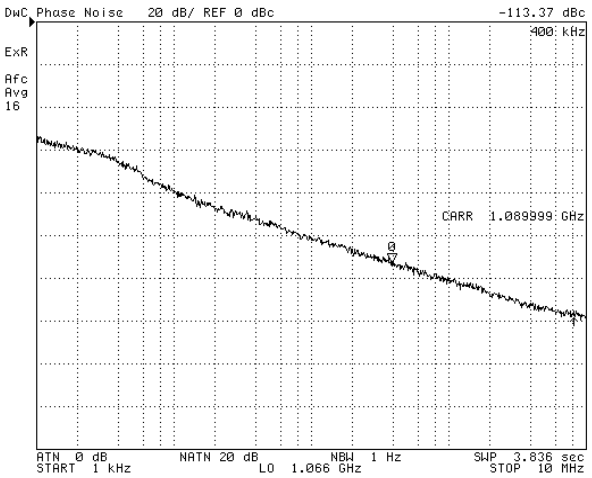

Fig. 7. Phase noise.

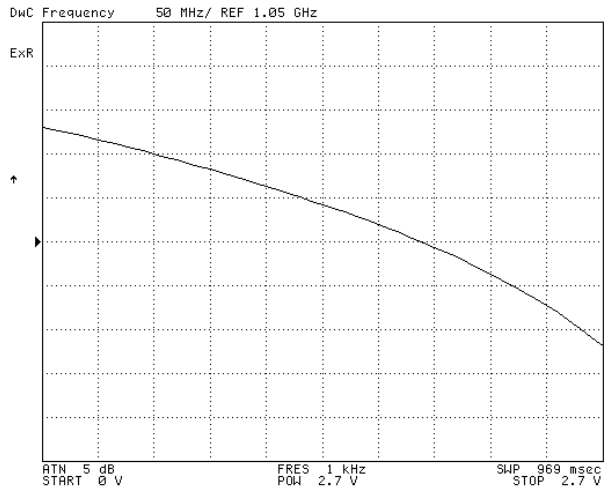

Fig. 8. Tuning Characteristics.

Characteristics	1 GHz VCO	0.5 GHz VCO
Technology	SOI BiCMOS	SOI BiCMOS
Supply Voltage [V]	2.7	2.7
VCO Supply Current [mA]	4	4
Buffer Supply Current [mA]	11	11
Output Level [dBm]	– 5.1	– 3.4
Frequency Tuning [MHz]	931 – 1180	415 – 543
Phase Noise @ 100 kHz	– 102	– 103
Phase Noise @ 400 kHz	– 113	– 114

Fig. 9. Summary of measurement results.