Challenges and Design Considerations for Integrated VCOs in Wireless Communications

Ken Suyama

Epoch Microelectronics, Inc.
220 White Plains Road, Suite 330, Tarrytown, NY 10591
E-mail: ken.suyama@epochmicro.com

Abstract

This paper attempts to list challenges and possible solutions for designing integrated voltage controlled oscillators (VCOs) in wireless products. Such challenges include oscillation frequency, frequency coverage, linearity of tuning curves, phase noise, power consumption, oscillation amplitude variations, sensitivity to process, supply voltage, and temperature variations (PVT), coupling to and from other blocks, start up time, and area. Some design considerations for voltage regulators are also discussed since the noise performance of such regulators can influence the overall design significantly. VCOs in CMOS processes are mainly considered here. An example of taking advantage of modern CMOS processes with active devices with different threshold voltages is also presented.

1. Introduction

Recent trend for RF receivers and transceivers for high volume market such as tuners, cellular phone, wireless LAN, etc. is moving toward complete integration of front-end blocks, frequency synthesizers, baseband blocks in a system on chip (SoC) using fine line CMOS technologies such as 65nm and beyond [1, 2]. Although fundamental design issues for VCOs are common to any generation of CMOS or BiCMOS processes, fine line CMOS processes present additional challenges such as higher 1/f noise, smaller headroom for VCO to swing, etc.

Various design issues and some known solutions are reviewed in this paper. Since modern CMOS technologies provide different device options, circuit designers can still be inventive to utilize them. One example of using MOS devices with different threshold voltages to make VCO tuning curve linear will also be presented.

2. Basic LC VCO Structure

In this paper, we consider LC based VCOs that consist of three main blocks, on-chip spiral inductor, a capacitor block with on-chip varactors and band-switching capacitors, and negative resistance (Fig. 1(a)). The negative resistance is often realized by cross-coupled PMOS devices, cross-coupled NMOS devices, or CMOS configurations (Fig. 1(b)). In most of wireless applications, a regulator is needed to stabilize the biasing either through self-regulating schemes [3] or separate regulating circuits. Although such a regulator can generate a stable DC condition with respect to supply voltage and temperature variations, it adds complexity to trade-offs among noise and start-up time as explained later (Sec. 6).

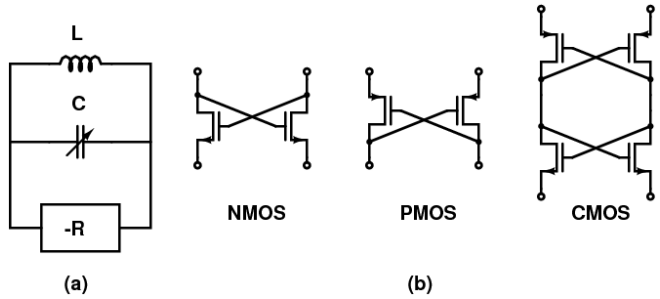

Fig. 1. Basic VCO structure and common form of negative resistance

A conceptual NMOS VCO (Fig. 2) will be used to illustrate various issues. The regulated VCO has 5 binary weighted coarse tuning bands and a fine tuning MOS varactor for achieving a specified frequency coverage. The coarse tuning is normally provided by MIM or MOS capacitors. The current through the LC tank can be adjusted by a 3-bit bias current control circuit so that the oscillation amplitude can be programmable.

3. Oscillation Frequency and Frequency Coverage

The oscillation frequency is determined mainly by the inductor L and the total capacitance that is the sum of the band switching capacitors and the fine tuning varactors.

As oscillation frequency gets higher, the effects of parasitic capacitance and inductance become significant. Therefore, careful post-layout parasitic extraction must be done to minimize unwanted frequency shift from the desired frequency range. An example showing tuning characteristics is shown in Fig. 3. The number of bands and the size allocation of capacitance among the varactors and band-switching capacitors are determined by considering many factors such as desired Kv, frequency coverage, overlap percentage of neighboring tuning curves, etc.

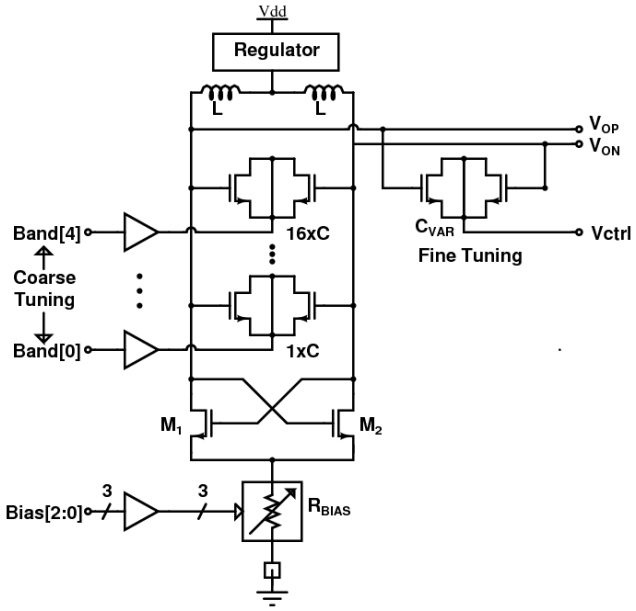

Fig. 2. A conceptual NMOS VCO circuit diagram

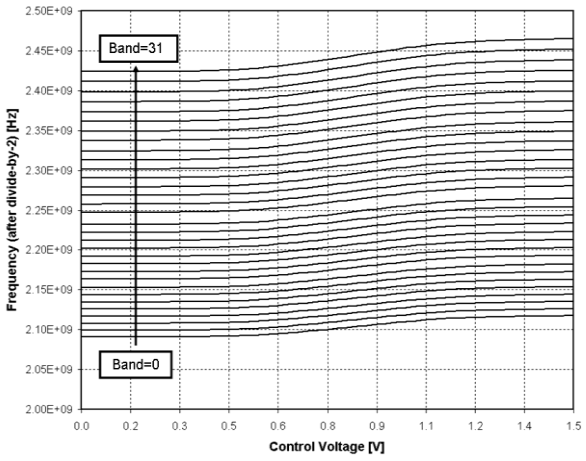

Fig. 3: An example of tuning curves of a 5GHz VCO with a 5-bit band switching capacitor array (after a frequency divider).

4. Supply Pushing

The supply pushing is defined as a change of oscillation frequency with respect to a change in the supply voltage ($\Delta f/\Delta Vdd$). The effect manifests itself by shifting tuning curves such as the ones in Fig. 3 up or down when the supply voltage changes. Some possible remedies are (1) to use a PMOS structure such that the PMOS varactors are reference to the ground and (2) to regulate the power supply. A common solution to the supply pushing problem in product design is to regulate the supply. The use of a regulator in VCO design, however, can add more complex trade-offs among phase noise and turn-on time as shown in Sec. 6.

5. Temperature Variations

Temperature mainly affects frequency tuning curves, oscillation amplitude, and phase noise performance. It is even necessary to consider the temperature coefficients of the loss of inductors that would affect not only the phase noise performance but also the robustness of oscillation (that is, oscillation can stop at some temperature range). An example of such frequency shift due to temperature change from -40C to +95C is shown in Fig. 4. Without any temperature compensation scheme, this particular VCO does not have enough frequency coverage per tuning curve to correct the frequency shift by changing the control voltage. If such a temperature drift is not acceptable, some temperature compensation scheme needs to be implemented.

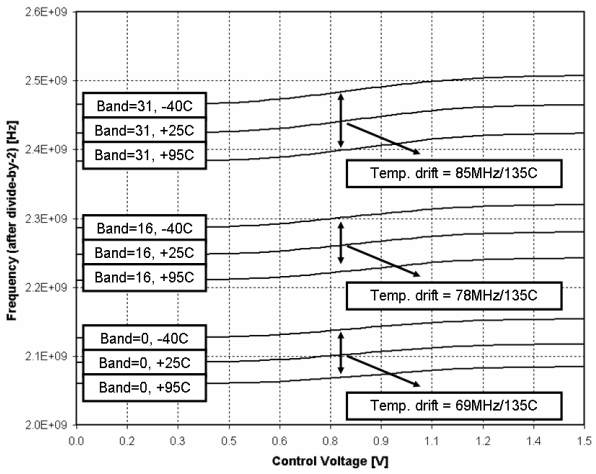

Fig. 4: An example of frequency shift (measured) due to temperature change.

A common temperature compensation scheme to reduce the frequency shift shown in Fig. 4 is to purposely embed a temperature dependence to the VCO control voltage such that the embedded temperature dependence cancels the original VCO temperature dependence [4-6].

For phase noise degradation over temperature, if the system is such that it is possible to change the tank current, changing the current through the programmable bias current to control the oscillation amplitude is one solution.

It should be noted that simulation of the temperature behavior of VCOs often does not match well with actual measurement. Therefore, some programmability needs to be designed into the whole system to avoid catastrophic failure.

6. Phase Noise and Regulator

Numerous papers have dealt with schemes and analyses to lower the phase noise of VCOs [for example, 7-12]. Common approaches are (1) to use PMOS cross-coupled devices, if possible, for lowering 1/f noise [12], (2) to maximize the oscillation amplitude but keeping the swing within current limiting region [8], (3) to use high Q passive elements as much as possible [7], (4) possible noise filtering [10,11] and (5) to use caution in layout. A trade-off between low-Q layout and low-parasitic capacitance layout needs to be checked carefully.

As mentioned in Sec. 4, a voltage regulator circuit is often used to minimize the supply pushing. A simplified band-gap circuit is shown in Fig. 5.

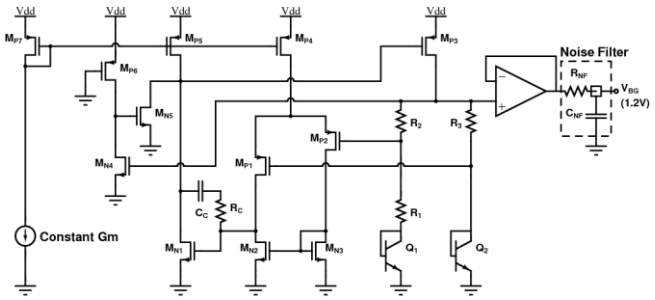

Fig. 5. A simplified band-gap circuit with noise filter.

One major drawback of the approach is that such a regulator generates noise that can be modulated up around the oscillation frequency to affect the VCO phase noise significantly. Common approaches to reduce the noise in the band-gap circuit are to adjust the ratio of diodes and to increase the current. More aggressive approach that is often used in product design is to apply a noise filter with a large time constant (*i. e.* a large capacitor). This, in turn, slows down the band-gap regulator to settle down to its final value. Thus, the startup time for the whole VCO becomes significantly long. There are solutions to this problem also such as a speedup scheme to charge up the large capacitor in the noise filter. Nevertheless, this illustrates the complexity of designing a robust VCO that can be used in a product.

7. Extending Linear Tuning Ranges [13]

Fig. 3 shows the nonlinear behavior of tuning curves due to the MOS varactors that are inherently nonlinear. PLL designs often require Kv to be within a certain ratio, for example 2:1. Therefore, the usable control voltage range is limited by the nonlinearity.

A linearization technique, often used in Gm-C filters [14-15], based on the superposition of several offset nonlinear transfer characteristics can be used. Recently, this linearization technique has been applied to linearize VCO tuning characteristics by offsetting accumulation varactors [6]. Since MIM-capacitors and accumulation varactors are not available in this particular process, the technique presented in [6] cannot be used directly.

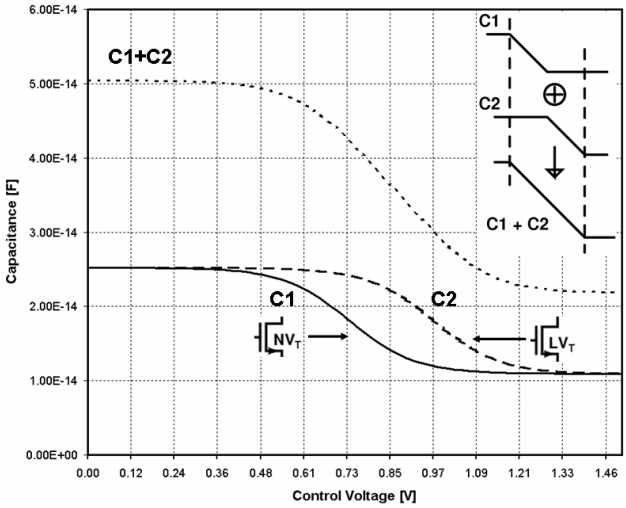

Fig. 6. Concept and simulation of linear range extension using two MOS capacitors with low and normal threshold voltages [13].

The inset of Fig. 6 shows the conceptual diagram for two offset nonlinear capacitances C1, C2, and the composition C1+C2. In theory, a linear tuning range of the combined C1+C2 varactor can be effectively doubled as compared to individual varactors C1 and C2. An implementation of this concept is to combine MOS inversion varactors with different threshold voltages. In modern CMOS processes, MOS transistors with several threshold voltages are often available. Fig. 6 also shows the simulated linear tuning range extension using normal threshold voltage (NV_T) and low threshold voltage (LV_T) transistors. The effectiveness of this approach is shown in

Fig. 7 where VCO tuning curves with NV_T+NV_T and NV_T+LV_T varactor combinations are compared. The NV_T+NV_T varactors based VCO shows a linear range of 360mV, whereas the NV_T+LV_T varactors based VCO shows a linear range of 500mV, which corresponds to a linear range extension of 38 percent. Since the offset mechanism is achieved with different MOS threshold voltages, no auxiliary bias circuits are needed, and therefore, any potential phase noise degradation due to the bias noise is avoided. Also, there is no penalty in the area and power consumption by using this proposed technique.

This illustrates that variety of options available in modern technologies [16] can give circuit designers tools to be creative to counter difficult design challenges.

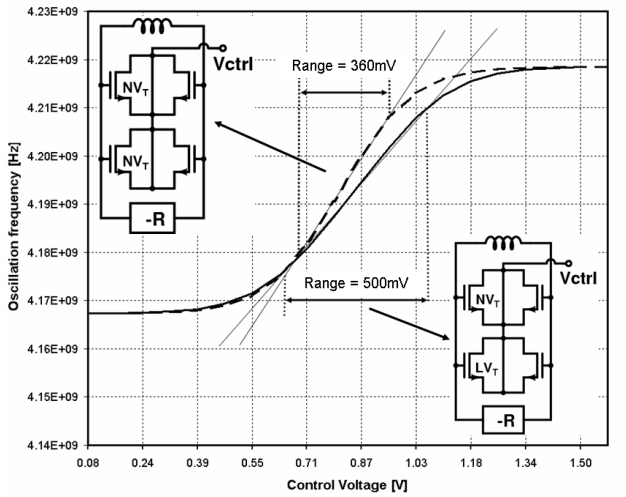

Fig. 7. Simulated rage extension for a VCO circuit [13].

8. Conclusions

Design issues and the review of known solutions for implementing integrated VCOs in modern CMOS processes are presented. Some of the trade-offs among a complicated inter-dependent set of parameters are identified. As an example, the relationship among a voltage regulator circuit, phase noise, and the start-up time of VCO has been explained. Modern technologies have many device options. Taking advantage of such a RF CMOS process where several MOS devices with different threshold voltage are available has also been illustrated. By using MOS devices with two different threshold voltages, it is possible to extend the linear region of a tuning curve without additional circuit.

9. Acknowledgment

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