A 10 GHz Frequency-Drift Temperature Compensated LC VCO with Fast-Settling Low-Noise Voltage Regulator in 0.13 μm CMOS

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Abstract - **This paper presents an LC voltage controlled oscillator (VCO) with an integrated compensation circuit that reduces oscillation frequency drift due to temperature variations. The temperature compensation circuit consists of MOS inversion varactor as a compensation capacitor, and BJTs and resistors for temperature dependent voltage bias generation, and noise contribution suppression of a bias noise. The effectiveness of this technique is demonstrated in a 10 GHz LC VCO with a frequency divider (divide-by-2), output measurement buffer, and integrated fast settling low noise voltage regulator. The VCO achieves current consumption of 21.0 mA, tuning range of 10.63 GHz to 12.33 GHz, phase noise of - 109.9 dBc/Hz at 1 MHz offset from 6.12 GHz carrier. The VCO frequency-drift due to temperature is improved by 82 % with the compensation circuit.**

I. INTRODUCTION

A temperature drift of VCO oscillation frequency is a critical problem for CDMA type applications where the synthesizer must remain locked over entire temperature range and cannot be re-locked [1]. It is possible to design such a VCO with a wide tuning range using single tuning band, where temperature drift is calibrated by adjusting the single tuning band control voltage of MOS devices as varactors [2] [3]. This implementation, however, is not suitable for monolithic integration due to high VCO gain and tuning nonlinearity. The high VCO gain has a high sensitivity of the noise coupled onto the control voltage. It can be viewed as frequency-modulation (FM) noise which up-convert low-frequency noise components in the control path to the frequency region around the carrier [4]. To minimize VCO phase noise through the FM noise mechanism, low VCO gain is preferred [5]. With a low VCO gain, the PLL may be un-locked by temperature drift of oscillation frequency once the control voltage exceeds the tuning range of the band under a condition that any band calibration is prohibited during normal operation. To reduce such a temperature drift, several integrated LC VCOs with temperature compensation techniques have been demonstrated [6] [7].

This paper presents a VCO frequency temperature drift compensation technique, which offers a low noise, a small current consumption, and no external components. It is implemented in a 10 GHz LC VCO design. The prototype integrates a frequency divider, measurement output buffer, and fast settling low noise voltage regulator for power supply.

II. PROPOSED TECHNIQUE

Figure 1 shows the proposed approach for frequency-drift temperature compensation. It consists of a voltage reference bias Vref generation stage, a switchable MOS inversion varactor array, and a temperature dependent voltage bias VTC generation stage. Vref is generated by a resistive voltage divider that consists of R4 and R5 to R8. R5 to R8 are among dominant noise sources. To suppress their noise contributions to the VCO's phase noise, Q3 is inserted where the voltage across Q3 act as a battery so that the value of R5 to R8 can be made smaller without increasing the current consumption. In order to minimize temperature variations of Vref, Q4 was inserted to track the temperature variation of Q3. 3-bit switchable MOS inversion capacitors MC1, MC2, and MC3 are connected in parallel to control a compensation capacitance contribution to the VCO tank capacitor. The temperature dependent voltage bias VTC is generated by the negative temperature coefficient of VBE characteristic of BJT. Two BJTs (Q1 and Q2) are connected in series to realize larger temperature dependency to VTC.

The C–V characteristics of MOS inversion capacitors used in the compensation circuit are shown in Figure 2. The total capacitance of the temperature compensation circuit is set by the bias voltage difference VTC – Vref. Since VTC decreases as the temperature increases, the total capacitance decreases as temperature increases. Therefore, it compensates VCO frequency tuning variation caused by the fixed tank capacitors whose capacitance increases as temperature increase.

A MOS inversion capacitor has strong process dependency as shown in Figure 2. It can be compensated by switching R5 to R8 at the Vref bias generation stage in Figure 1. For example, when process comes out faster, a larger resistor value can be selected to compensate a smaller transistor threshold voltage.

III. CIRCUIT DESIGN

A 10 GHz LC VCO is designed to demonstrate the effectiveness of the temperature compensation varactor on the VCO tuning curve performance. The schematic of the

VCO is shown in Figure 3. The 10 GHz LC VCO is implemented in a complementary cross-coupled differential topology to achieve common-mode supply and substrate noise rejection, and low phase noise with high power efficiency. To minimize the supply pushing and frequency modulation of any noise on the voltage supply of the VCO, a regulated VCO power supply is used. To reduce noise effect through the control voltage to the phase noise, we chose VCO gain to be low [5]. Inductors L2 and L3 are inserted to provide a high reactance for the NMOS and PMOS switching pair to avoid the transistors entering the triode region and degrades resonator's quality factor. This, in turn, prevents phase noise degradation [8].

To provide large frequency coverage with a small VCO gain, 7-bit binary-weighted MIM capacitor array as coarse tuning is used for sufficient frequency overlap.

MOS inversion capacitors are used as varactor for the fine frequency tuning. This is because accumulation varactors were not available in this process. To avoid the varactors enter into the accumulation region and induces sudden capacitance changes when the signal at the transistor gate is large, the MOS bulk terminal is grounded [9].

All MOS inversion varactors including the compensation capacitors are implemented in a differential fashion to maximize the quality factor [10]. A 3-bit programmable resistor array controls the current through the VCO, and is used for post fabrication current and phase noise optimization.

This VCO is implemented into a test chip as shown in Figure 4. The VCO is followed by a conventional CML divider [11] and a 50 ohms measurement output buffer. For today's modern communication systems, I/Q modulations are mandatory and their I/Q LO signal can be generated with high accuracy by quadrature devide-by-2 circuits and it relaxes some of the direct-conversion architecture design issues such as self-mixing of RF and LO signals [12]. A low-noise fast settling voltage regulator is used to generate 2.3 V and 1.8 V regulated supplies for the VCO circuit, and the divider and output buffer circuits, respectively. To achieve low noise, the bandgap noise is filtered using an RC filter with a large off-chip capacitor C1. To ensure a fast turn-ON time and fast settling, one shot circuit is used on power-ON to enable a class-AB buffer for a few microseconds. The class-AB buffer then quickly charges up the external capacitor to the bandgap voltage. When one shot pulse returns to zero, the class-AB buffer is disabled and the regulator operates in its default low noise mode.

IV. MEASUREMENT RESULTS

The temperature compensation varactor, 10 GHz LC VCO, divider, buffer, and voltage regulator circuits were fabricated in a 0.13 μm CMOS process. The VCO layout is shown in Figure 5. The chip has been packaged in a QFN64 package and was mounted on a conventional FR4 device evaluation board. All measurements were done using Agilent 5052B Signal Source Analyzer.

Figure 6 shows the measured tuning characteristic for all 128 bands after divide-by-2 at room temperature. The measured tuning range is from 5.34 GHz to 6.20 GHz, which corresponds to a VCO tuning range of 10.68 GHz to 12.40 GHz.

The measured VCO gain after the divide-by-2 at room temperature is shown in Figure 7. The peak VCO gain varies from -75 MHz/V to -110 MHz for band 0 to 127, respectively, which corresponds to -150 MHz/V to -220 MHz/V at the VCO output. The lower VCO gain at low band setting is caused by the cross-coupled CMOS pair parasitic, which constitutes a significant portion of the tank capacitance [13].

Figure 8 shows measured VCO frequency over temperature from -30 C to 125 C with and without the temperature compensation at BAND = 64. VCO gain is - 87.8 MHz / 1.5 V and - 94.3 MHz / 1.5 V with and without the compensation, respectively, at T = 25 C. The maximum frequency variation over temperature change with compensation is - 10.5 MHz from T = -30 C to 85 C, whereas the maximum frequency variation without the compensation is - 61.6 MHz from T = -30 C to 125 C at Vcont = 0.75 V. This can be translated into a frequency tuning variation improvement from 65 % to 12 % in a band with Vcont from 0 V to 1.5 V by a charge pump in a PLL loop.

A measured supply pushing at divide-by-2 is shown in Figure 9. The worst case supply pushing from 3.0 V to 3.6 V supply variation is 380 kHz, which corresponds to 760 kHz/0.6V at the VCO output.

Measured phase noise after divide-by-2 is shown in Figure 10. The worst case phase noise is -109.9 dBc/Hz at 1MHz offset from 6.12 GHz carrier frequency at room temperature. The phase noise variation from -30 C to 125 C is less than 1 dB.

The VCO circuits consume 21.0 mA from the regulated 2.3 V supply.

V. CONCLUSION

An LC VCO with integrated temperature compensation MOS inversion varactor circuit has been demonstrated in 0.13 μm CMOS process. The effectiveness of the proposed temperature compensation has been confirmed by measurements where the maximum VCO oscillation frequency-drift from -30 C to 125 C is improved from - 61.6 MHz to - 10.5 MHz by applying the compensation circuit.

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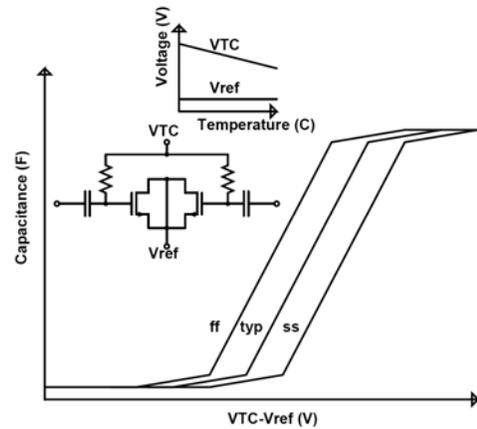[13] B. Razavi, "A 1.8GHz CMOS voltage-controlled oscillator," *ISSCC Dig. Tech. Papers*, pp. 388-389, February 1997.

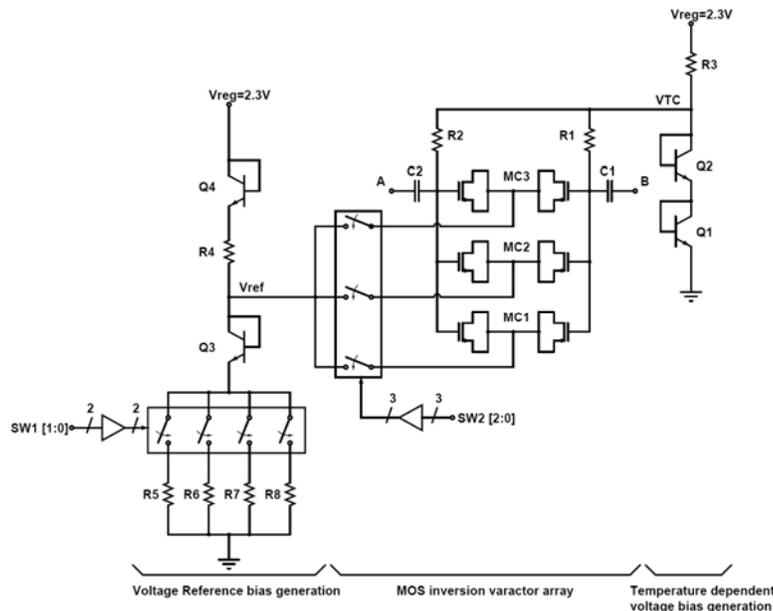Fig. 2. MOS inversion capacitor behavior of the proposed temperature compensation circuit.

Fig. 3. Schematic of the 10 GHz LC VCO.

Fig. 1. Conceptual diagram of proposed temperature compensation MOS inversion varactor.
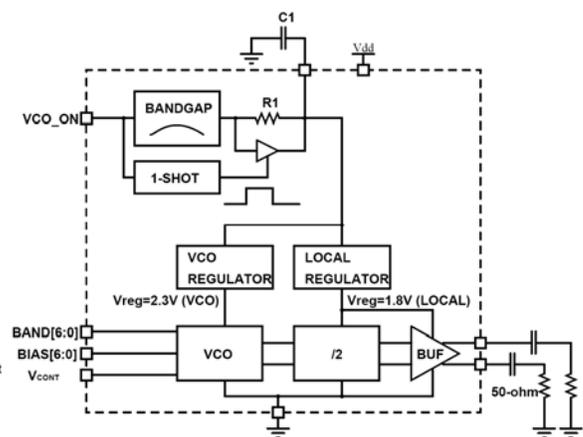

Fig. 4. Block diagram of the VCO test chip.
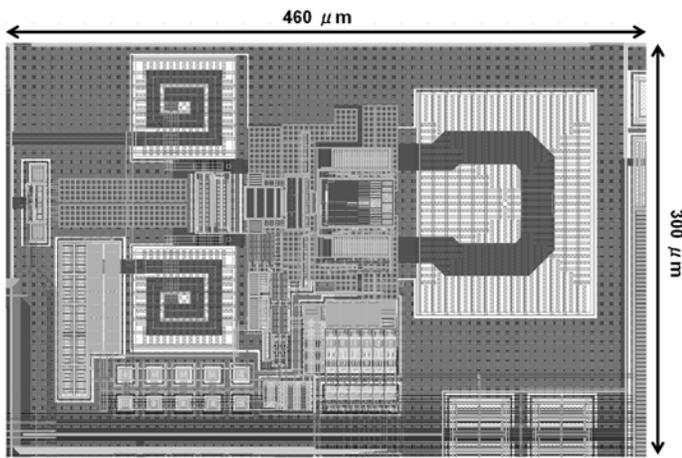
Fig. 5. Layout diagram of the proposed LC VCO.

Fig. 8. Measured frequency drift at BAND = 64 (after div / 2).
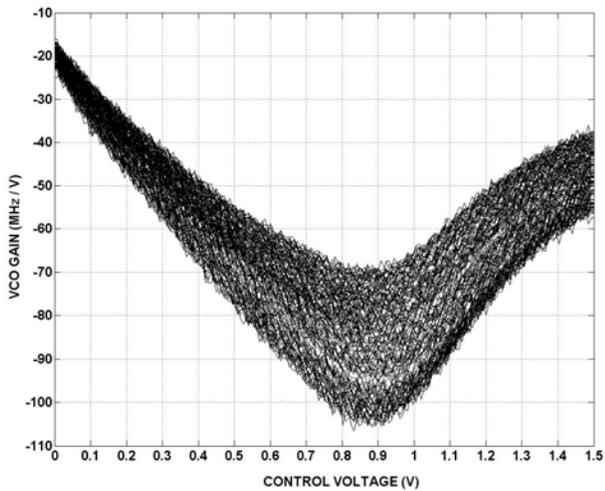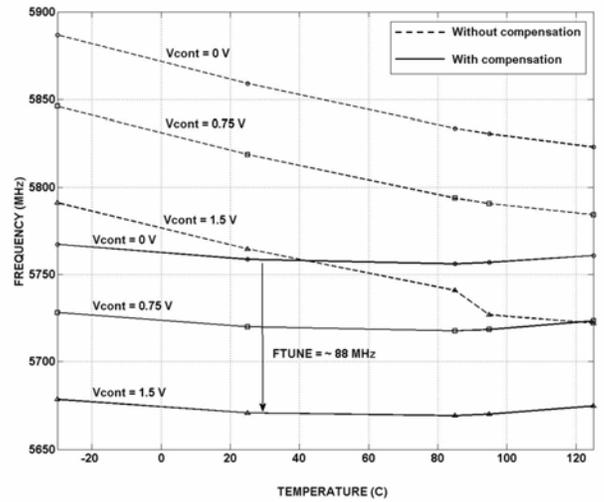

Fig. 6. Measured frequency tuning (after div / 2).

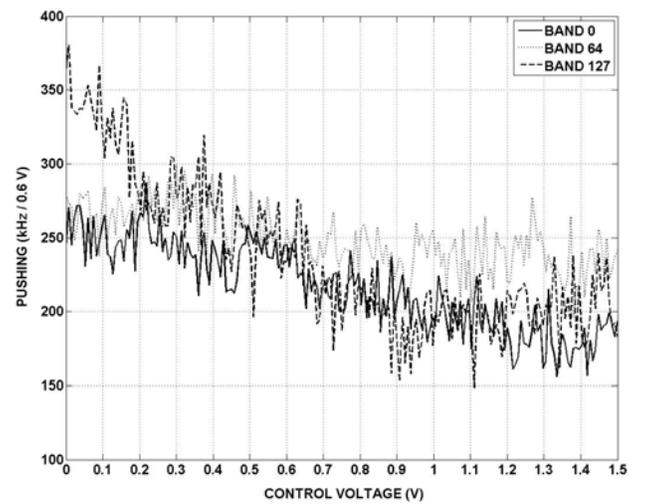Fig. 9. Measured supply pushing (after div /2).
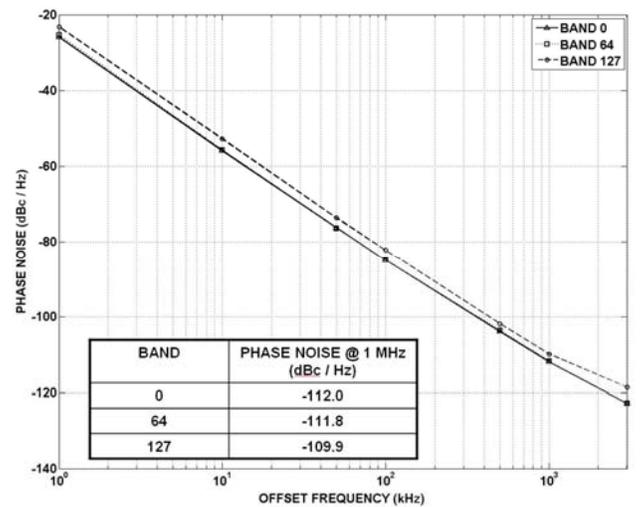

Fig. 7. Measured VCO gain (after div / 2).

Fig. 10. Measured phase noise at Vcont = 0.75 V (after div / 2).